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Non-volatile memory and negative photoconductivity in a metal-insulator-semiconductor diode with embedded Co nanoparticles

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We describe a new metal-insulator-semiconductor (MIS) device in which cobalt based nano particles (NPs) in a core-shell structure (Co–core and Co_3O_4-shell) are embedded between a thermally grown SiO_2 layer and a HfO_2 film deposited by atomic layer deposition. Two additional structures were prepared for comparison. One had no NPs and the other included the Fe NPs, prepared using the same procedure as used for the Co film. All devices exhibited the classic behavior of a voltage variable MIS capacitor with or without a large hysteresis as in non-volatile memory (NVM) systems. However, only the device with the Co core-shell structure exhibits a negative photoconductivity (NPC) effect as well as NVM capabilities in both the capacitance-voltage (*C-V*) and current-voltage (*I-V*) characteristics. The dependence of *C-V* and current voltage *I-V* characteristics on illumination intensity and wavelength (from ultraviolet to near infrared) as well as on temperature was characterized. Illumination enhances the NPC effect as well as the flat-band voltage shift determined from C-V characteristics and hence the memory width. Illumination in the wavelength range of 735–780 nm caused a current decrease, at a given voltage, by up to a factor of two. The NPC effect stimulates an annihilation of the stored charges and therefore erases the system instantly at a small applied bias. The main cause of the NPC effect under illumination is the photo excitation of supplementary trap channels in the Co_3O_4 shell, which lowers the free carrier density and hence the conductivity of the MIS structure. *Published by AIP Publishing.*
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I. INTRODUCTION

Significant progress was achieved in recent years in non-volatile memory (NVM) metal-insulator-semiconductor (MIS) capacitors based on semiconductor[1–6] or metallic nanoparticles (NPs).[7–14] Metal NPs with large work functions such as Au, Pt, and Co have been used as floating gates in an NVM system fabricated on bulk Si or Si-on-insulator substrates.[7,8,10–13,15–18] Such metal NPs have larger charge-storage capacity and this leads to memory windows and retention times which are significantly larger than in structures that use semiconductor NPs.[1–6] This is due to the deeper potential wells and the ability to accurately control the size and distribution of metal NPs.[8,16–18]

The effect of illumination was reported in Refs. 18–20, where it was shown that illumination widens the memory window, speeds up the response, and yields improved retention properties. Illumination increases the density of minority carriers due to photo generation in the depletion regime and therefore impacts the charge state of the metal nanoparticles. In photoconductors, this phenomenon is known as a positive photo conductance (PPC) effect. In contrast, MIS structures fabricated on p-Si substrates, where the SiO_2 film[2] or an SiO_2/HfO_2 stack[4] were implanted by Si or Ge nanoparticles, exhibited some shrinking of the memory window in the capacitance-voltage characteristic (*C-V*). Also, a photo current reduction was observed under illumination at a forward bias. This effect was explained by transport of photo generated electrons from the Si NPs to the Si substrate, causing the NPs to be positively charged and hence they screened the applied voltage. This resulted in a reduction of the majority carrier (holes) penetration through the insulator so that the net current was reduced. Stored charge elimination and negative photoconductivity (NPC) were observed also in MIS structures based on an n-Si substrate, containing an insulator stack with embedded Ge nanocrystals.[3] An effect similar to that described in Refs. 2 and 4 was explained by negatively charging, under forward bias, of the Ge NPs by photo generated electrons. Negatively charged NPs prevent the penetration of majority carriers (electrons) from the n-Si surface resulting in a decrease in the total current.

NPC was also observed in several materials such as bulk Si doped by Au[21] or Co.[22] It was explained by the formation of deep acceptor and donor centers in the band gap of the semiconductor. Under illumination, simultaneous excitation of these levels [forming donor (acceptor) like traps and recombination of excited electrons (holes) from the conduction (valence) band] are common factors which result in NPC in bulk semiconductors.[23] NPC in Si-implanted bulk

GaAs which was initially doped by Cr was also observed.[24] The transformation of the photo ionized deep impurity levels to effective traps enhances the probability of the majority carrier recombination rate and therefore the net current reduces relative to that in the dark. Extremely high NPC was found in modulation-doped GaAs/AlGaAs quantum wells at low temperatures due to an illumination induced reduction of the majority-carrier mobility by electron-hole scattering.[25,26] NPC in polycrystalline ZnO grains[27] or nanowires[28] was attributed to the capture of excited carriers in the conduction band of ZnO, by states distributed at the grain boundaries or traps in an aluminum oxide layer covering nanowires, with energy larger than the ZnO band gap. NPC in graphene[29] was shown to result from the loss of illumination excited carriers by oxygen ions. Finally, in Ref. 30, NPC was observed for the first time in a system of Au and Ag nanoparticles surrounded by self-assembled monolayer (SAM) thin films. The NPC effect was related to initial capture by the NP cores of free carriers, which were then excited by illumination to the polaron-like states in organic ligands of SAM and trapped there. The process exhibited leakage current reduction relative to the dark regime.

This paper reports on an extensive study of p-Si based MIS diodes where the insulator comprises a stack of SiO_2 and HfO_2 in which NPs having a core-shell structure are embedded. The core is Co while the shell is Co_3O_4. Co has a large work function, about 5.0 eV (Ref. 31) so that the work function difference between the NPs and Si provides a deep potential well of about 0.95 eV which offers, in turn, better carrier confinement in the potential well[7,8,18] in comparison to semiconductor (Si or Ge) NPs. The MIS structure reveals both NVM and NPC properties which are vastly enhanced compared to previously reported alternatives.[2–4] The core-shell structure enables hysteresis (and hence memory functionalities) in the current-voltage (*I-V*) (in addition to the *C-V*) characteristics. This was not observed previously with any other NPs. The spectral response of the device covers the range of ultra-violate to infra-red. We describe the dependence of both *I-V* and *C-V* characteristics on wavelength and illumination intensity as well as temperature.

II. EXPERIMENTAL PROCEDURE

A. The structure of the MIS capacitors

The structure we studied comprised a double layer NVM capacitor fabricated on a P type Si (100) substrate with a doping concentration of 8×10^{15} cm^{-3}. A 3.0 nm thick thermal SiO_2 tunneling layer of thermal SiO_2 was covered with a 0.8 nm Co layer which underwent rapid thermal annealing (RTA) in a forming gas. A 20 nm thick HfO_2 blocking layer was consequently deposited by atomic layer deposition (ALD) at 350 °C. Hafnium tetra-chloride and water were used as precursors. During the RTA process, the Co film transform into nanoparticles by the process of dewetting, while the ALD process yields a core shell system where the Co is a core and the Co_3O_4 (which is a high band gap semiconductor[32]) acts as the shell. The gate electrodes were made of Ti/Au and had an area of 5.0×10^{-4} cm^2 while Ti/Au/Al was used for the back electrodes. Two additional structures were prepared for comparison. One had no NPs and the other included Fe NPs which were prepared using the annealing procedure as for the Co film. The diodes contained the same insulator sublayers as the main structure. *I-V* characteristics measurement was performed using an Agilent 4155C semiconductor parameter analyzer, while *C-V* and impedance-voltage (*Imp-V*) curves were measured with an HP4192A LF impedance analyzer and an MDC7200 capacitance meter at 1 MHz. Light emitting diodes at 365 nm to 880 nm wavelengths were used to illuminate the devices by means of a lensed fiber that provided a spot area of 7.35×10^{-3} cm^2. High resolution transmission electron microscope (HRTEM) micrographs of the cross section and an energy-dispersive spectroscopy (EDS) mapping of the elements were obtained in a double corrected and monochromated Titan Themes microscope operated at 300 kV and using dual-X detectors.

III. RESULTS AND DISCUSSION

A. Structural image, EDS mapping, and magnetic properties of the MIS structure

Figure 1(a) shows a scanning electron microscope (SEM) image of round Co NPs with small separations average sizes of 5–10 nm. Figure 1(b) illustrates a HRTEM cross section image of the structure with details of the sublayers. Figure 1(c) shows an EDS mapping of the metal Co and oxygen. While the Co core is not distinguished clearly from the oxygen included area, the figure reveals an obvious intensity gradient between the central dark areas and its surrounding blue background (see also the inverse contrast of the EDS mapping of the metal Co). We postulate therefore that Co NPs are embedded into the oxygen included shell material. EDS mapping of the Co nano-crystalline sheet shown in inset Fig. 1(b) is an additional demonstration of the real form of the partially separated NPs, similar to what is shown in the SEM image [see Fig. 1(a)].

The superparamagnetic properties of the MIS structure were measured by a vibrating sample magnetometer and are illustrated in Fig. 2. The dependence of the magnetization curves shows no hysteresis at room temperature. The observed superparamagnetic characteristics resemble those discussed in Refs. 33–36 for cobalt oxide (Co_3O_4) NPs, which were synthesized at a moderate temperature of 250 °C as well as at temperatures above 400 °C. The magnetic properties of Co_3O_4 are sensitive to the shape and size of the NPs.[34] It was shown in Ref. 34 that Co_3O_4 NPs with sizes larger than 10 nm exhibit no coercivity (absence of a hysteresis) above the critical temperature of 4 K with zero magnetic field cooling, in agreement with the superparamagnetic nature. For NPs smaller than 10 nm, the critical temperature increased and reached 12 K for a diameter of 3 nm. An analogous result was reported in Ref. 35. Note that the presence of the Co core can also cause a shift of this value to higher temperatures. The small volume of each nanoparticle results in a crystalline anisotropic energy barrier that is smaller than the thermal energy. Therefore, at room temperature, the particles are naturally demagnetized. Annealing in an oxygen atmosphere at temperatures above 300 °C yields Co_3O_4 (Refs. 37 and 38) or Co-Co_3O_4 (core-shell) structures.[39,40] In light of

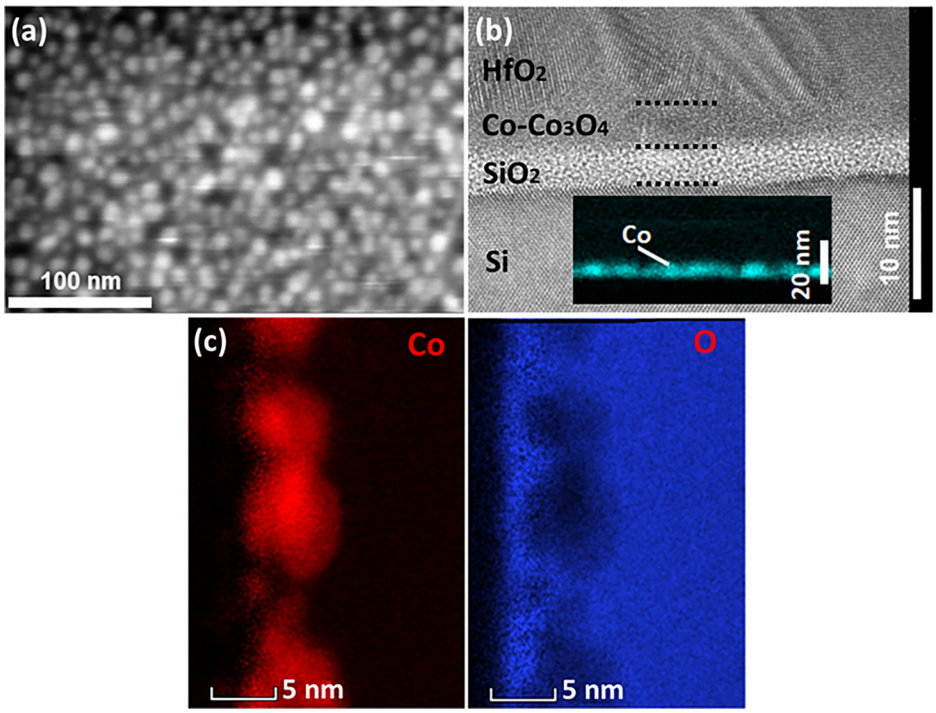

FIG. 1. (a) SEM plan view image of the Co NPs after the RTA process, (b) HRTEM cross section image of the structure, and (c) EDS mapping of Co NPs and oxygen taken in the same area. Inset of the EDS mapping of the Co nano-crystalline sheet.

this, and with support of the EDS mapping, we conclude that the ALD deposition of the HfO_2 top layer dictates similar conditions to those described in Refs. 37–40 where a Co-Co_3O_4 compound is formed from a thin film crystallized Co that underwent a RTA process.

Among the various cobalt oxide configurations (Co_2O_3, Co_3O_4, and CoO), Co_3O_4 has the most stable phase and is hence known to have many practical applications.[41,42] It is a valence p-type semiconductor; a mix of CoO (Co^{2+}) and Co_2O_3 (Co^{3+}), with a spinal structure, where Co^{2+} and Co^{3+} cations are placed at tetrahedral and octahedral sites, respectively.[32,41,43,44] In Co_3O_4 (as in most transition metal oxides), the *d*-electron orbitals of metal cations are partially filled and are split between the valence and conduction bands. The valence band is influenced by filled d-d orbitals of both cobalt oxidation states and by O-2*p* orbitals of the oxygen anion. The conduction band is mostly formed from empty d-d orbitals of both cations. The conduction in normal spinal structures mainly occurs through electron excitation (by thermal or optical means) from the oxygen ligand to the metal cation, which is defined by a charge transfer band gap. The influence of the transition from the *d-d* ligand to each of the Co^{2+} and Co^{3+} cations in normal spinel structures is small.[45] Several peculiarities of the electrical characteristics of the device we studied are interpreted assuming the presence of Co_3O_4 crystalline inclusions.

B. Room temperature current-voltage characteristics in dark and illumination regimes at different wavelengths

Room temperature *I–V* curves measured in the dark and under illumination at 365 nm and an illumination power density (P_L) of 4×10^{-4} W/cm^2 are shown in Fig. 3(a). For comparison, Fig. 3(b) shows the *I-V* characteristics of a MIS structures with similar insulator stacks, but uses Fe NPs or without them (see inset). What distinguishes the present device from other MIS diodes having no[46] [see also inset in Fig. 3(b)] or containing metal NPs such as Au[47] or Fe is the fact that under reverse bias, the current in the dark is more than two times larger which is a clear indication of negative photo conductivity. It is similar to what was reported for MIS NVM structures with embedded semiconductor NPs.[2,4] However, there are several distinct differences including: (i) NPC is observed only for bias levels that induce depletion in the semiconductor and not in the accumulation regime. (ii) The ratio of dark to illumination current is larger here than that reported in Refs. 2 and 4.

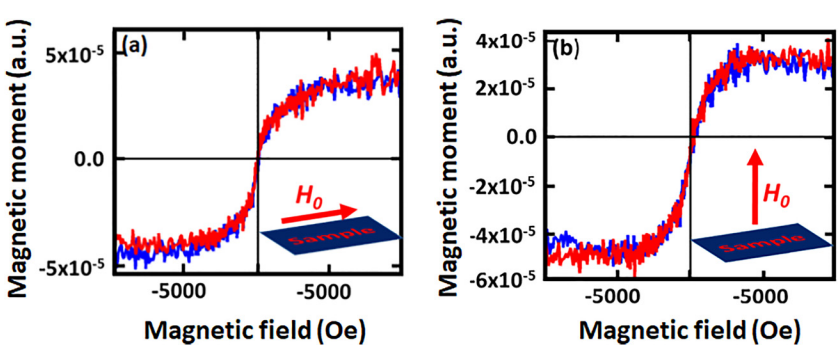

FIG. 2. Room temperature measurements of the normalized magnetic moment versus magnetic field for the MIS structure with the embedded Co. (a) In plane and (b) out of plane. The arrows indicate the directions of the magnetic field.

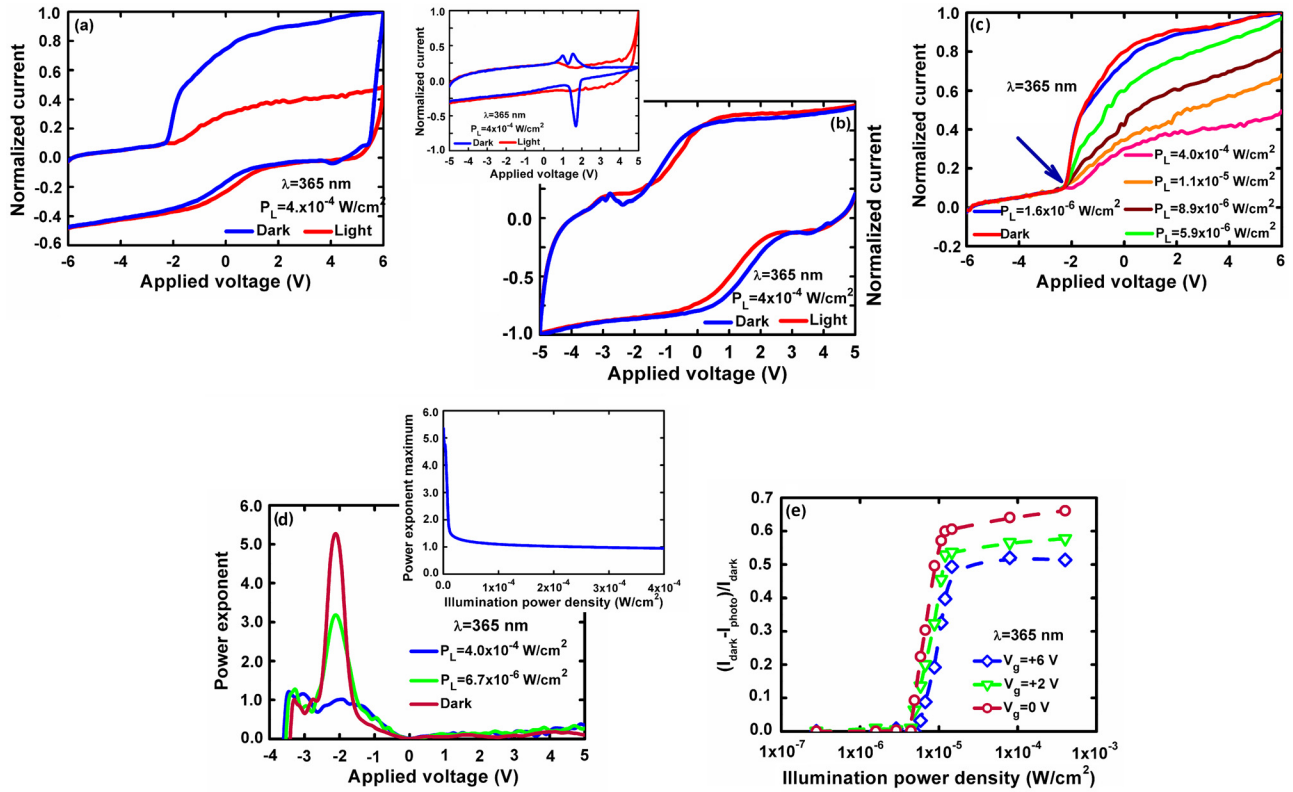

FIG. 3. (a) Normalized *I-V* characteristics of the MIS structure with Co NPs measured in the dark and under illumination. (b) Normalized *I-V* characteristics of the MIS structure with Fe NPs measured in the dark and under illumination. The inset shows, for comparison, similar characteristics for a structure containing no NPs. (c) *I-V* dependence on illumination power density. (d) β-*V* characteristic dependence on illumination. The inset shows the dependence of the maximum value of β on illumination power density. (e) The $(I_{dark} - I_{photo})/I_{dark}$ ratio dependence on illumination power density.

Figure 3(c) describes *I-V* characteristics measured from the negative to the positive voltage direction under illumination at 365 nm for different illumination power densities. The *I-V* characteristics were transformed to the power exponent formalism $\beta = dln(I)/dln(V) = (V/I)(dI/dV)$,[48] the resultant β-*V* characteristics, shown in Fig. 3(d). Figures 3(c) and 3(d) reveal three distinct regions. In the ranges of -6 V to -3 V and zero to $+6$ V, the *I-V* curves are saturated ($\beta \ll 1$) for all illumination conditions. In the dark, near the point which separates dark and photocurrent (indicated by an arrow), a super linear dependence is observed which translates to a maximum in the β-*V* curve. Under illumination, the *I-V* characteristics change their slope in this region so that the maximum in the β-*V* curves reduces. For large illumination powers, the characteristics become essentially linear and β approaches unity [see the smooth maximum in Fig. 3(d)]. The change in the maximum β value with illumination power is described in the inset of Fig. 3(d).

The current ratio $(I_{dark} - I_{photo})/I_{dark}$ measured at different positive voltages is shown in Fig. 3(e). In the range of dark to $P_L = 2.7 \times 10^{-6}$ W/cm^2, the current changes very little. A similar behavior is observed above 4.1×10^{-5} W/cm^2. Between these regimes, illumination has a strong influence where larger illumination reduces the photocurrent. In a narrow region of power, from 5×10^{-6} W/cm^2 to 1.4×10^{-5} W/cm^2, the current ratio increases linearly with the illumination intensity, when the applied gate voltage (V_g) varies from zero to $+6$ V.

The *I-V* characteristics are also affected by the illumination wavelength. This is shown in Fig. 4(a) where for all wavelengths, the density is held constant at 4.1×10^{-6} W/cm^2. The dependence on the wavelength of the ratio $(I_{dark} - I_{photo})/I_{dark}$ is shown in Fig. 4(b); at short wavelengths, the ratio is low. It increases with the wavelength, reaches a weak maximum at 735–800 nm, and then reduces. The effect of wavelength changes on the β-*V* curves shown in Fig. 4(c) resembles the effect of illumination power density changes [see Fig. 3(d)].

The super linear character of the dark *I-V* which yields a large β value, cannot be caused by contribution of interfacial traps in the thermionic emission process.[49,50] In that case, β is a linear function of the applied voltage without a maximum in the β-*V* curves.[50,51] The discontinuity in the leakage current in the dark and under low illumination power can be interpreted in terms of a space charge limited current (SCLC), while the maxima in the β-*V* curves can be interpreted as a trap filling voltage, when traps are completely filled by holes or electrons. In the dark, oxygen vacancies were located at the boundary of the Co NPs and surrounded by the HfO_2 blocking sublayer (formed during the RTA and ALD processes) play the role of the traps. These vacancies result from breaking Hf-O chemical bonds.[52,53] Moreover, when the blocking layer is grown on top of the metal NPs, the initial atomic layers of the HfO_2, covering the NPs, grow as a porous rather than a continuous film,[54,55] with a large stoichiometric deficiency of oxygen.

The drop of the β-*V* curve beyond its maximum can only be induced by contact limited emission current, often

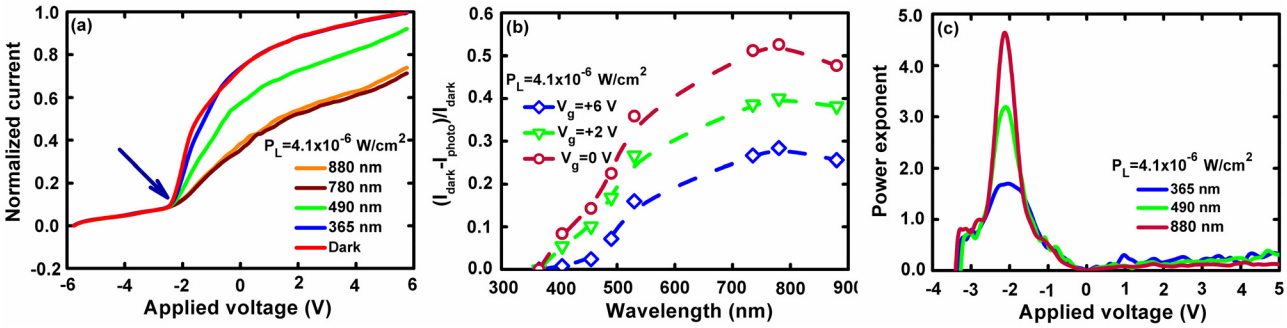

FIG. 4. (a) Wavelength dependence of the normalized *I-V* characteristics at a constant illumination power density. (b) Wavelength dependence of the $(I_{dark} - I_{photo})/I_{dark}$ ratio at different gate voltages. (c) Power exponent versus applied bias for different illumination wavelengths.

revealed following the SCLC regime.[56] This is the limiting case of the SCLC regime at high bias due to the non-virtual but constant level of the contact emission.[57] The latter means that the external field does not heat the carriers appreciably within the region of their mean free path between the contact surface and the semiconductor bulk.[58]

The lowering of the power exponent with illumination intensity is also a well known experimental fact, which was discussed in the literature in the context of wide band gap photoconductors with deep trap levels.[56,59,60] The deep levels, which in the dark are filled, can be exited (charged) by illumination and act as new traps for the injected carriers. The limitation of the electrodes to act as virtual sources of carriers makes it difficult to fill the exited traps before beginning of the contact emission limited current regime and hence causes a reduction in the rate of current rise with voltage.[56,59,60]

C. Temperature dependence of the I-V characteristics

Temperature dependent *I-V* characteristics in the range of 223 K to 292 K are shown in Fig. 5. Figure 5(a) is for the dark regime and Fig. 5(b) represents measurements under illumination at 365 nm with a constant illumination power density of 5.2×10^{-5} W/cm^2. The measurements used zero stress time t_{stress} for the negative start voltage (V_{start}) which scans in the positive voltage direction. In the dark, the current changes by more than an order of magnitude above 223 K while under illumination, the dependence on temperature is comparatively very weak. In Fig. 5(c), the temperature dependence of the leakage current in dark at two voltages values $V_g = +1.5$ V and $+3$ V are demonstrated as conventional $ln(I) = f(1/kT)$ plots.[61] The estimated activation energies can be extracted easily, $E_{act} = 0.26$ eV and 0.28 eV, respectively, at $V_g = +1.5$ V and $+3$ V. The fact that under illumination the variation of E_{act} is almost temperature insensitive ($E_{act} \cong 0.02$ eV) testifies to the fact that the photo carriers totally dominate the thermally generated carriers, in contrast to the dark regime where the temperature plays a significant role.

D. The origin of the negative photoconductivity

The observed NPC effect is assumed to result from charge process enhancement in trap sites which are exited under illumination.[27,28,30] Such trap sites can be produced during the RTA and ALD processes when the Co oxidizes to form Co_3O_4 or Co (core)-Co_3O_4 (shell) compounds.[32,40,43,62] Measurements of the dependence on photon energy ($h\nu$) of the absorption coefficient (α) of Co_3O_4 films and analyzing the $(\alpha h\nu)^2$ versus $h\nu$ function yields a linear fit, typical of direct interband transitions in semiconductors. Two allowed direct optical band gaps at 1.4 to 1.7 eV and at 1.88 eV to 2.3 eV are revealed.[37,40–42,44,61–65] The low optical energy was identified as a sub band located inside the energy gap, while the large one corresponds to an inter band transition associated, respectively, with O^{2-} to Co^{3+} and O^{2-} to Co^{2+} charge transfers. The wide variation of optical transition energies reported in the literatures is evidently caused the differences in fabrication methods and the resulting sizes of the nanoparticles. The low sub band energy was associated with the acceptor level (E_A),[37,42,61] which is located below the conduction band edge. As the density of the holes in p-type Co_3O_4 is above 3×10^{18} cm^{-3},[42,61] the Fermi level is close to the valence band edge (controlled by shallow acceptor levels). Therefore, the aforementioned deep acceptor

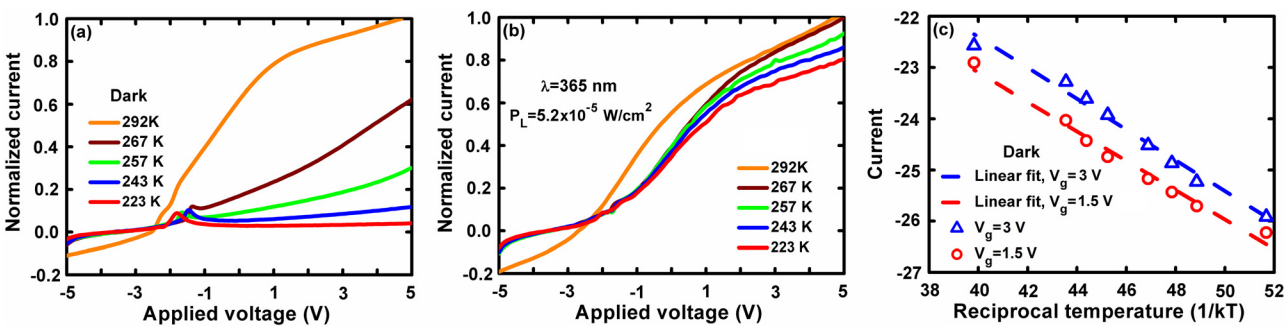

FIG. 5. Temperature dependent *I-V* characteristics. (a) In the dark. (b) Under illumination. (c) Leakage current, in logarithmic units, versus reciprocal *kT*, measured in the dark.

level in the dark regime is essentially not populated by the electrons exited from the valence band at any temperature. In accordance with Refs. 37, 42, and 61, the difference of the conduction band and sub band energy depends on the fabrication process of forming the Co_3O_4 compound and varies from 0.21 eV to 0.54 eV. These values are related to the activation energy (E_{act}) extracted from temperature dependent conductivity or leakage current and in p-type semiconductors is approximately given by the energy difference from the conduction band, $E_A = 2E_{act.}$[61] The activation energy, 0.26–0.28 eV, was obtained above from the temperature dependence of the leakage current [Fig. 5(c)] and hence $E_A = 0.52$–0.56 eV which is close to those reported in Refs. 37, 42, and 60. The value of $h\nu = 1.59$–1.69 eV (735–780 nm), at which the maximum NPC effect is observed [see Fig. 4(b)], can also be identified with the energy level of deep acceptors relative to the valence band edge of the Co_3O_4 compound.[37,40–42,44,61–65]

Possible transformation of the metal Co sublayer into the Co-Co_3O_4 nano crystalline compound with deep acceptor traps, assumes the applicability of the mechanism of realization of the NPC effect suggested in Refs. 27, 28, and 30. Illumination-induced reduction in leakage current at a positive bias (when the device is swept from accumulation to depletion/inversion) can be attributed to the loss of the photo generated electrons injected toward the reverse biased (positive) gate electrode. However, unlike carriers in the dark regime, photo electrons are captured not only by traps inside the Co (core) NP potential well, but they are also captured by deep acceptor levels of Co_3O_4 directly or after penetration into the conduction band and following recombination. The spectral dependent of the ratio $(I_{dark} - I_{photo})/I_{dark}$ [see Fig. 4(b)], which is small at a short wavelength and reduces above 780 nm is different than the PPC characteristics of photo detectors based on the Si substrate. The small difference between dark and photo current at short wavelengths is a result of a large absorption coefficient of the bulk Si substrate similar to PPC. However, the reduction at wavelengths longer than 780 nm is not related to the absorption properties of Si, but to an insufficient energy of the photons to excite injected electrons to be captured by the deep acceptor level in the band gap of the Co_3O_4 compound. In contrast, the reduction of the PPC in Si based photodetectors occurs at around 900 nm.

E. Capacitance-voltage and impedance-voltage characteristics in dark and illumination regimes at different wavelengths

Normalized high-frequency *C-V* and *Imp-V* characteristics of the memory structure with Co NPs at a sweeping voltage that changes gradually from depletion to accumulation and vice-versa are shown in Figs. 6(a) and 6(b). These curves were measured in the dark at room temperature. Figures 6(c) and 6(d) show *C-V* and *Imp-V* characteristics under illumination and for a constant sweeping voltage.

Rightward and leftward shifts of the *C-V* characteristics (hence a flat band voltage shift) with increasing sweeping voltage are, respectively, due to negative charging by electrons (minority carriers) generated in the Si depletion region or positive charging by holes (majority carriers)[49,66,67] of the Co NPs or of the traps in the Co based compound. Figures 6(a) and 6(c) reveal that the initial and shifted curves are parallel which indicates a uniform distribution of the trapped charges. The dependences of the flat band voltage shift (ΔV_{FB}) on the voltage sweep and hence of the memory window width defined by the *C-V* characteristics in both bias polarities are summarized in Fig. 6(e). The horizontal axis indicates the absolute value of the applied voltage. In order to estimate the values of ΔV_{FB}, we compare V_{FB} to its neutral value (V_{FBN}) which is determined, in turn, from *C-V* curves that are measured at the smallest possible sweep voltages (± 1 V). The hysteresis widths (ΔV) measured at a sweeping voltage of ± 6 V are 5.3 V and 6.2 V, respectively in the dark and under illumination. The total charge density trapped in the Co or Co-Co_3O_4 sites at both bias polarities can be calculated, by using experimentally extracted ΔV, $N_{charge} = \frac{\triangle V C_{acc}}{qS}$,[1] with q being the electron charge, while C_{acc} and S are the accumulation capacitance and gate electrode area, respectively. At gate voltages, ± 6 V, and a capacitance density $C_{acc}/S = 4.9 \times 10^{-7}$ F/cm^2, N_{charge} is roughly 1.62×10^{13} cm^{-2} in the dark and 1.9×10^{13} cm^{-2} under illumination.

The *Imp-V* characteristics shown in Figs. 6(b) and 6(d) are correlated with the *C-V* curves; the extremum points coincide with flat band variation with sweeping voltage and illumination power density. In the dark, the hysteresis is related to the charging process of the Co NPs while under illumination, carriers exited in the Si depletion layer dominate over the thermally generated ones.[68,69] After injection toward the insulator stack, these carriers can be additionally captured by the deep traps in the Co_3O_4 compound. Therefore, the net hysteresis width of the *C-V* characteristics increases.

C-V measurements were also performed on devices with Fe NPs and without nanoparticles [see Figs. 6(f) and 6(g), respectively]. This observation testifies to the importance of the Co core-shell and Fe NPs in having a large memory window in both the dark and illumination regimes. A sweeping voltage of ± 6 V yielded a minor hysteresis of less than 0.5 V in Fig. 6(f). The small hysteresis and rightward shift of the *C-V* curves are the result of trapping/de-trapping at defects near the SiO_2-HfO_2 boundary or inside the HfO_2 film.[70,71]

The large shift in the positive bias direction of the flat band voltage, and hence the hysteresis width of the *C-V* and the absence of a shift to the negative bias region proves that illumination affects only the minority carriers (electrons). The difference between the conduction and valence band offsets of the tunneling SiO_2 layer, with respect to the silicon band edges, which are 3.2 eV for electrons and 4.6 eV for holes[72] also plays a role since electron injection is more efficient compared to hole injection. This is demonstrated in the inset of Fig. 6(c) which shows the shift in V_{FB} with illumination intensity. It increases in a conventional manner for positive bias but is basically constant for negative bias. The widening of the *C-V* hysteresis (about 1.2 V) is significantly smaller than in structures with the same dielectric stack grown under similar conditions, but which use Au[19,47] or Pt[18] NPs.

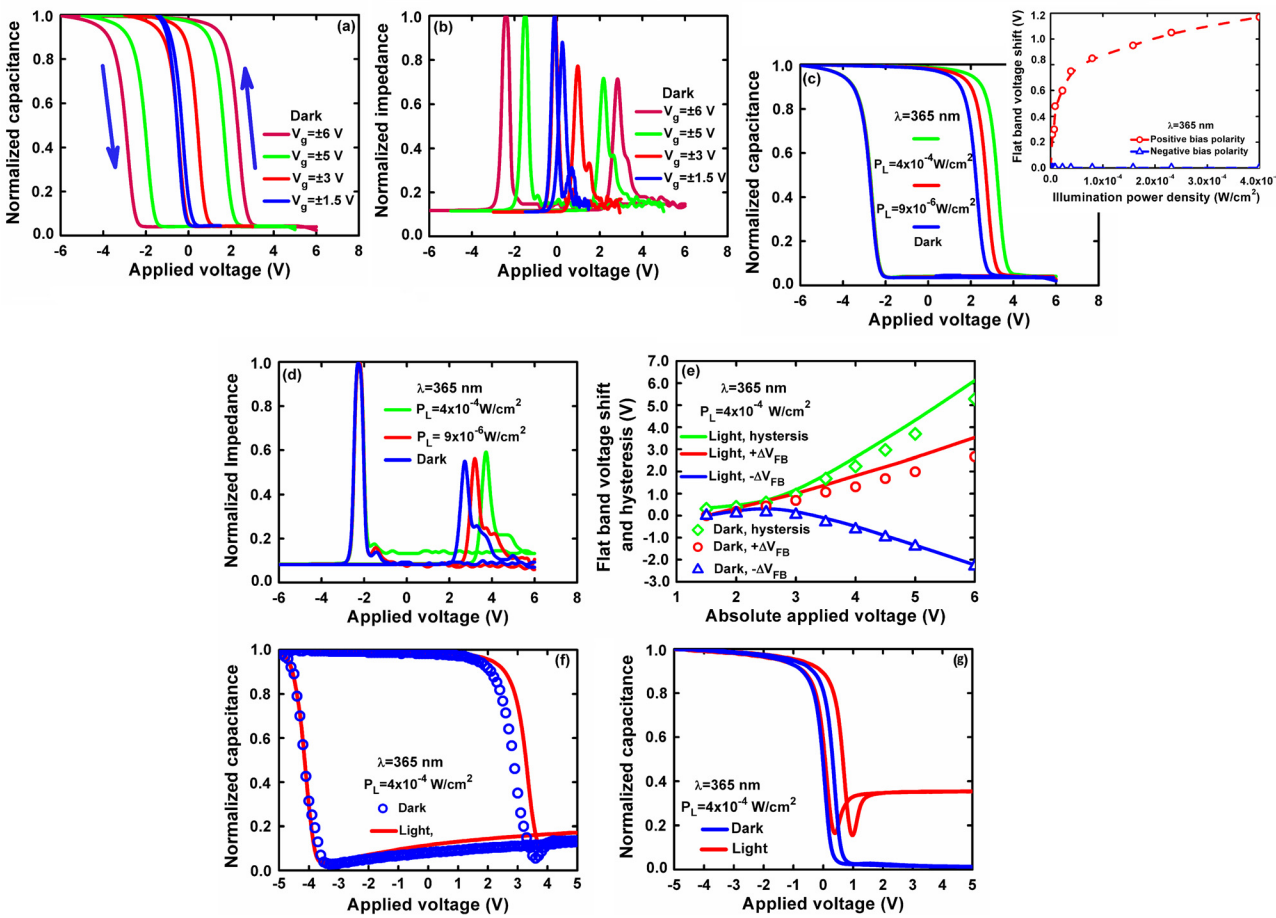

FIG. 6. (a) Normalized *C-V* and (b) *Imp-V* characteristics measured in the dark for different sweeping voltages. The arrows in (a) denote the clockwise direction of the hysteresis loops. (c) Normalized *C-V* and (d) *Imp-V* characteristics measured for different illumination densities. The inset in (c) shows illumination power density dependences of the flat band voltage shift for positive and negative bias. (e) Flat band voltage shift measured at negative and positive bias and the hysteresis width versus V_g in the dark and under illumination. (f) Normalized *C-V* characteristics of a MIS capacitor Fe NPs and (g) with no NPs measured in dark and under illumination.

F. Temperature dependence of the C-V characteristics in dark and illumination regimes

The *C-V* dependence on temperature, in the dark and under constant illumination at sweeping voltages of ±5 V is described in Fig. 7. In the dark [Fig. 7(a)], the *C-V* characteristics shifts depend on the applied voltage polarity. This is particularly so for temperatures below 292 K, where the flat band voltage shift for positive bias exhibits a large decrease as the temperature is reduced, while for the negative bias branch it is essentially unchanged. The temperature

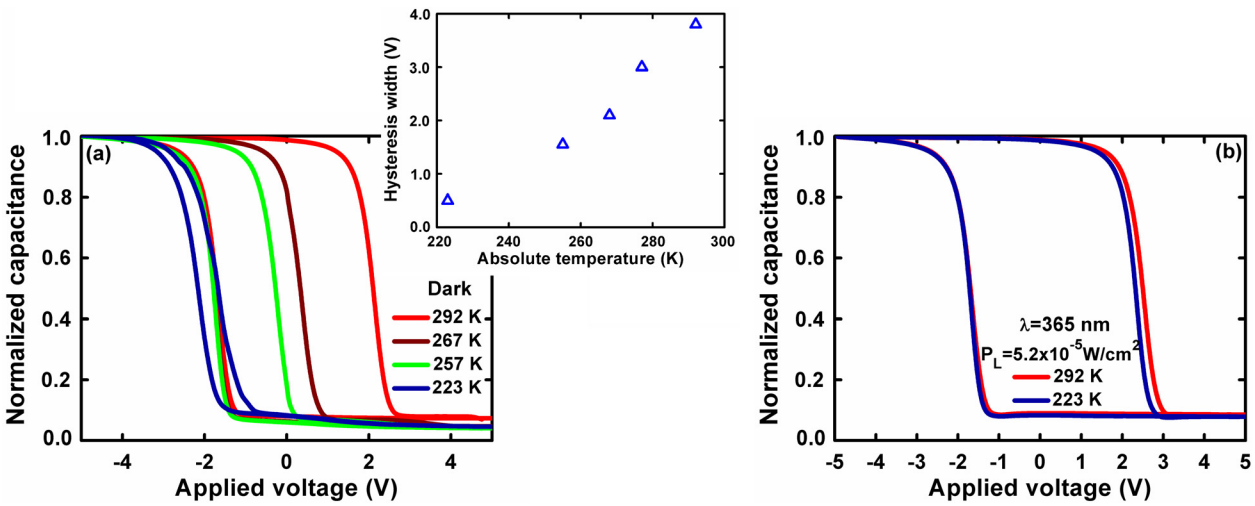

FIG. 7. Normalized *C-V* characteristic variation with temperature. (a) Measured in the dark. The inset shows the temperature dependence of the hysteresis width. (b) Measured under illumination.

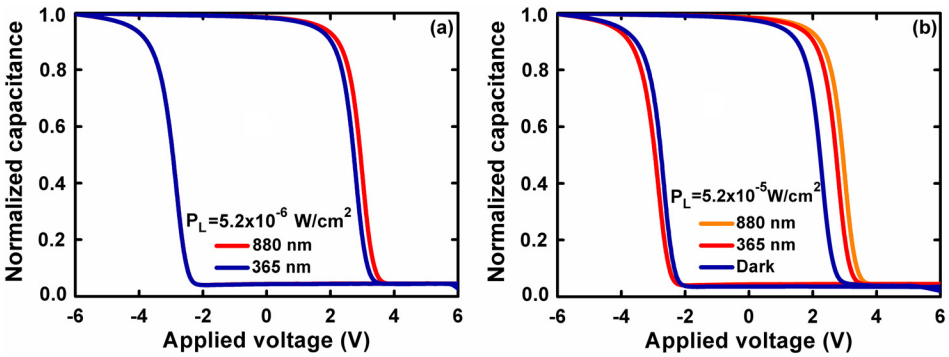

FIG. 8. Wavelength dependence of the normalized *C-V* characteristics. (a) Measured under low illumination power density. (b) Measured for an illumination power density which is one order of magnitude higher.

dependence of the total memory window width, shown in the inset of Fig. 7(a), indicates a super linear increase from 0.3 V at 223 K to 3.80 V at 292 K.

The results of Fig. 7(a) establish the fact that temperature and illumination affect similarly the shift of the *C-V* curves. Both determine the generation of minority carriers and their injection and eventual trapping by the NPs but illumination plays a larger role. For example, at 223 K, where the hysteresis width in the dark is only 0.3 V, even at an intensity of 5.2×10^{-5} W/cm^2 increases the width to 4.05 V, which is larger by 0.25 V than the dark width at 292 K. The total stored charge density in the dark was determined to be 9.2×10^{11} cm^{-2} and 1.13×10^{13} cm^{-2} at 223 K and 292 K, respectively, while under an illumination power of 5.2×10^{-5} W/cm^2, it increases to 1.24×10^{13} cm^{-2} at 223 K and then saturates.

The *C-V* dependence on wavelength at a low, 5.2×10^{-6} W/cm^2 illumination power, in 365 nm to 880 nm ranges is described in Fig. 8(a); the figure reveals the minor change with wavelength relative to dark. Figure 8(b) describes the behavior relative to the dark at the two extreme wavelengths, 365 nm and 880 nm, but under a larger illumination power, 5.2×10^{-5} W/cm^2. The observed difference is about 0.42 V and 0.6 V relative to the dark regime, respectively, at 365 nm and 880 nm. However, we note that these values are significantly smaller than for other metal NPs.[18,19,47]

G. The influence of the stress voltage on the carrier charging process and NVM like behavior of I-V characteristics

Prior to any *I-V* measurement, the device has to undergo a voltage stress process. The gate electrode is fed by a negative voltage (V_{stress}) for $t_{stress} = 15$ s. Furthermore, this voltage was used as a starting point (V_{start}) for the sweeping process. The initial bias was changed from −6 V to zero in 1 V intervals. The final V_g level was always +3 V. After completion of a single measurement, a constant erase voltage (V_{erase}) of +6 V was applied for erase time $t_{erase} = 15$ s in order to remove the charges accumulated by the traps during the previous process. This procedure was repeated for several V_{stress} and V_{start} values.

A set of *I-V* characteristics measured in the dark is shown in Fig. 9(a). An increase in the absolute value of V_{stress} shifts the curves to the negative voltage side with the curves being parallel to each other. The maximum is 5.2 V, obtained at $V_{stress} = -6$ V. This value was estimated by comparing the voltages corresponding to the current discontinuity in Fig. 9(a). Figure 9(b) shows the dependence of the estimated shifts on the start negative voltage which is linear.

At a fixed negative V_{stress}, majority carriers (holes) are attracted to the silicon-insulator interface forming the accumulation layer. These carriers are injected toward the negative biased gate electrode. However, some of the injected holes are trapped by the Co NPs and defect states, while others penetrate through the blocking HfO_2 layer and reach the gate electrode, creating a leakage current. The trapping processes results in an accumulation of positive charges on the NPs, which causes the shift of the *I-V* characteristics to the negative voltage direction in a similar manner to the effect seen in the *C-V* curves [see Figs. 6(a) and 6(e)]. This shift is completed at the flat band voltage. A reduction of the absolute value of the negative bias yields fewer positive charges on the NPs and other traps. At $V_{stress} = V_{start}$ equal to −5 V and −6 V, the current discontinuities are,

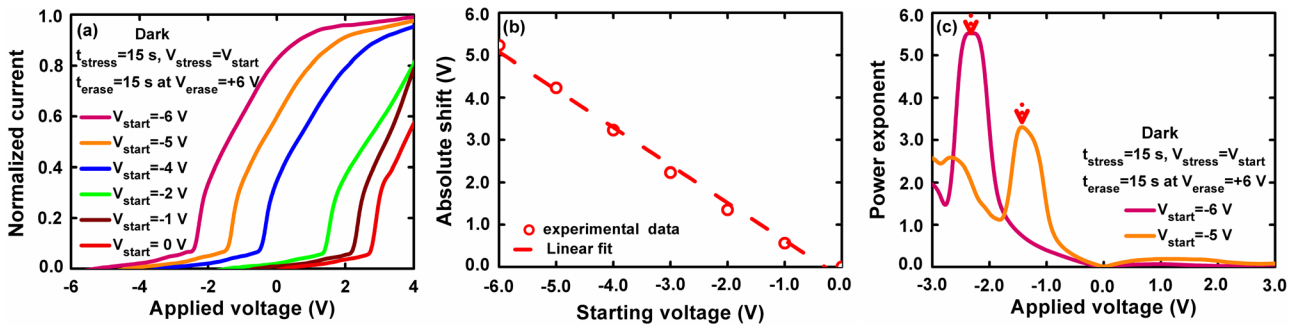

FIG. 9. (a) The shift of the normalized *I-V* characteristics with stress voltage for a constant stress time. (b) Absolute voltage shift for different V_{stress} at a constant leakage current. (c) The change of the β-*V* characteristics with stress voltage. The arrows denote the maximum β value.

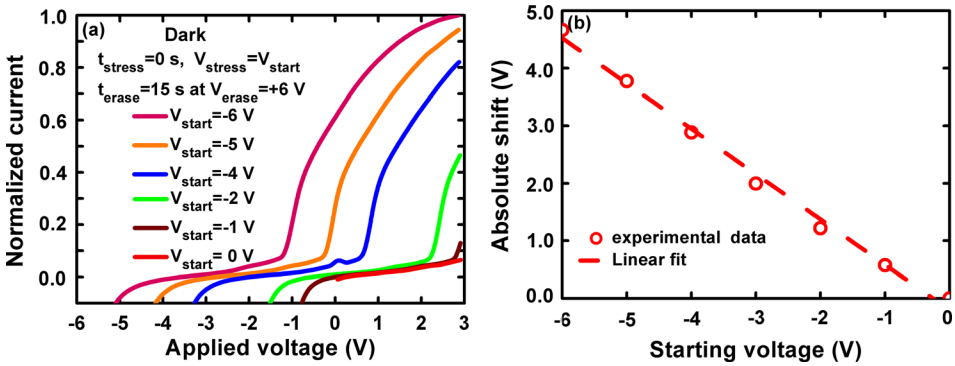

FIG. 10. (a) The shift of the normalized *I-V* characteristics with negative start voltage for a zero-stress time. (b) Absolute voltage shift with V_{start} at constant leakage current.

respectively, at −1.5 V and −2.6 V, which are close to the flat band voltages determined in the *C-V* curves. A more accurate value of the discontinuity voltage is determined from the maxima in the *β-V* characteristics shown in Fig. 9(c), which coincide with the *Imp-V* extrema [see Fig. 6(b)]. As the sweeping directions from negative to positive reaches flat band conditions, a transformation from the accumulation to the depletion regime takes place. In this situation, the NPs are neutral, allowing more leakage current to flow through the insulator stack, as seen in the *I-V* characteristics where a leakage current discontinuity appears. At absolute starting negative voltages below the voltage used to erase the accumulated positive charges, the shift of the *I-V* characteristics to the positive bias side is larger for voltages larger than −4 V. This leads to a difference of the bias levels where the discontinuity and the maximum *β* occur compared to the values extracted from the flat band voltages in the *C-V* characteristics, which are measured using a symmetric sweeping voltage.

The set of curves shown in Fig. 10(a) have been measured at the same conditions as in Fig. 9(a), but for $t_{stress} = 0$ s. Figure 10(b) illustrates once more, the shift of the voltage where the current discontinuity takes place as a function of V_{start}. The linear character is maintained, but the curves are shifted to the positive voltage side. The effect of t_{stress} on the shift of the *I-V* characteristics for a constant V_{start} of −6 V is described in Fig. 11 for t_{stress} of 0–15 s. The inset summarizes the shift magnitude dependence of the hold time. Unlike its linear dependence on the start voltage, the shift saturates at about 10 s.

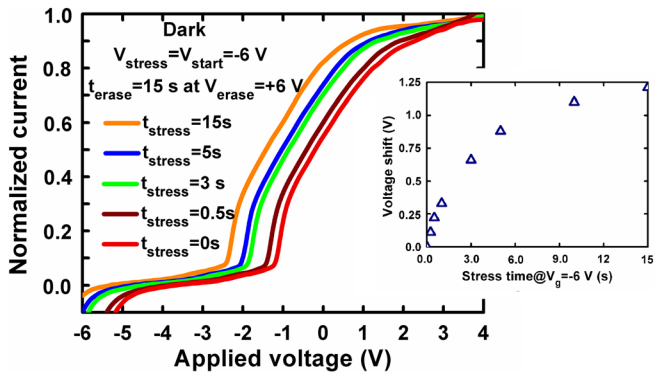

FIG. 11. Normalized *I-V* characteristics shift with stress time. The inset shows the voltage shift dependence on stress time at a constant leakage current.

We conclude that variation of V_{stress} and t_{stress} values control the current magnitude (the amount of charge trapped on NPs) and therefore the device operation, similar to the effect of the write voltage and duration in NVM systems. The erase procedure at positive voltages for a particular time is also similar to that of NVMs. The influence of these parameters on the *I-V* characteristics in the case of the illumination also is similar. However, the main role of the illumination in NVM application of is the possibility to instantly remove captured charges from the traps. The erase time is limited by the response of the carriers to different wavelengths and illumination powers.

H. Retention characteristics

Changes in the *I-V* characteristics due to varying start voltage and stress times denote, as in the *C-V* case, the influence of Co NPs or other defects to be charged. It is important therefore to examine the current based memory capabilities and compare them to what is possible using the capacitance. Figure 12 shows the preservation of charges accumulated in the Co NPs sites due to a negative stress voltage of −6 V lasting for $t_{stress} = 15$ s. The *I-V* curves were measured in the −1 V to +3 V range, at zero s, after 600 s and finally after 7200 s. The *I-V* characteristics shift with increased time in a parallel manner in the positive voltage direction. The current change with retention time, measured at different voltages relative to the initial ones, are shown in Fig. 12(b). The capacitance-time characteristics (*C-t*) are shown for the comparison. Capacitance and current are reduced with time; the leakage current reduction depends on the constant applied voltage, at $V_g = +3$ V, the reduction is roughly18%, while at $V_g = +0.25$ V it increases to 28%. The *C-t* characteristic at zero bias behave similarly, consistent with other non-volatile memory structures[18,20,73,74] using semiconductor or metallic NPs as a trap sites. The fast and slow drop of capacitance with time is related to losses of charges from trap sites due to several reasons: back tunneling to the semiconductor and lateral redistribution and trapping by defects formed at the NPs boundary with surrounding blocking or tunneling layers. The slow decay is due to the loss of charges through the blocking layer, assisted by traps related to oxygen vacancies.

The largest current reduction is close to zero voltage (a drop of 28% at $V_g = +0.25$ V compared with 18% at $V_g = +3$ V) is caused by different current mechanisms that take place at different regions of the *I-V* characteristics

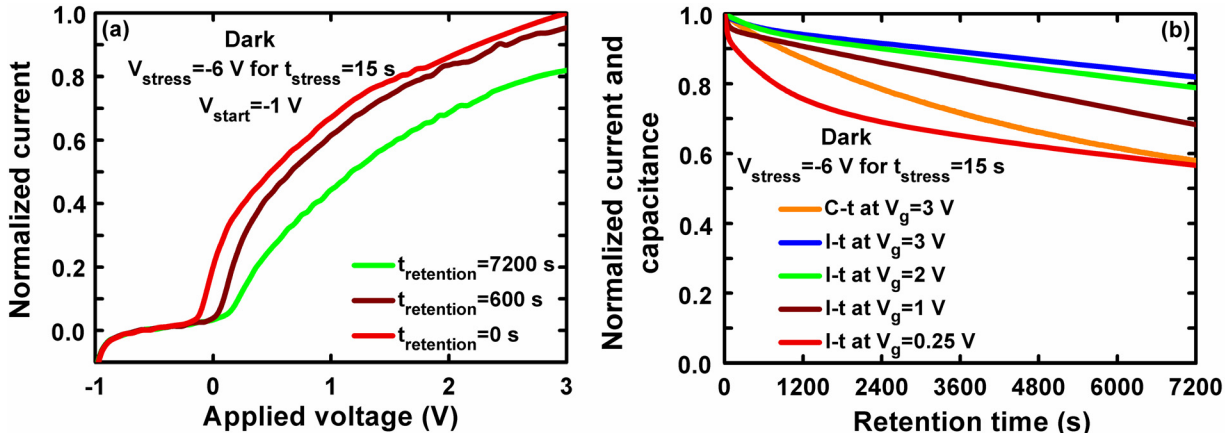

FIG. 12. (a) The shift of the normalized *I-V* characteristics with retention time. (b) Temporal evolution of the capacitance and leakage current at different gate voltages.

namely, a super linear behavior at low voltages and saturation at high bias levels. Thus, the memory capability in the *I-V* characteristics of this two-terminal diode is analogous to the drain to gate voltage characteristics of three terminals field effect transistors and hence the device we present can be used as a NVM. A special feature of this memory cell is the almost fast erase functionality obtained by illumination which is several orders of magnitude shorter than the conventional erase time (by voltage) in the dark.

I. Transient characteristics

Figure 13 shows the transient leakage current characteristics in response to a pulsed optical signal. A clear NPC is seen, similar to the static case (shown by dash lines) but with a very fast response under both turn on and turn off conditions. The *I-V* characteristics were measured with a 5 s and 10 s delay (t_{delay}) between the light and dark regimes. The response in both the turn on and turn off transient exhibits large over shoots which means that the NPC is much larger than in the static case.

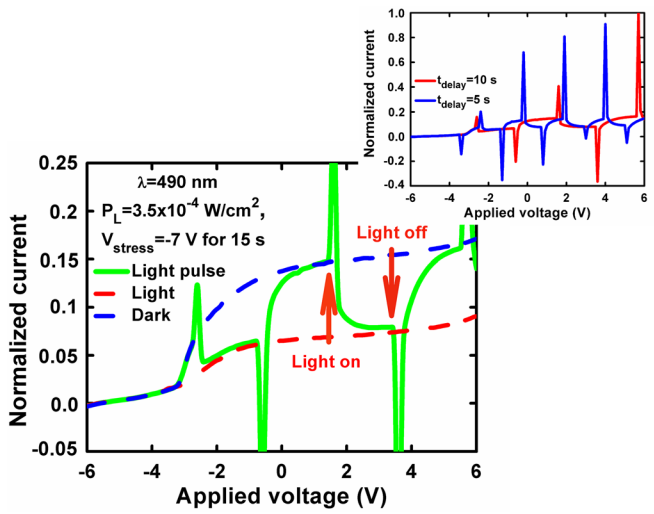

FIG. 13. Comparison of normalized static and transient *I-V* characteristics in response to a pulsed optical signal. The inset shows the transient leakage current versus applied voltage measured under pulsed optical signal with different delay times.

Such an effect has been observed in semiconductor based systems with different metal dopants,[75,76] that form deep levels in the semiconductor bandgap. Analogous with Ref. 77, we postulate that photo generated electrons in the conduction band of Co_3O_4 are captured by deep acceptor trap sites. The process is somewhat slow and therefore, there exists a short time window when the photo current increases sharply (this is the PPC effect). When illumination is turned off, carriers are no longer exited from the valence band. Before equilibrium is established, the conductivity reduces and a sharp NPC occurs. This is shown in Fig. 13. The inset illustrates the real deviation of the sharp peaks of both effects measured at delay times of 5 and 10 s.

IV. CONCLUSION

To conclude, we have demonstrated NPC and NVM behavior in MIS structures with embedded Co core and Co_3O_4 shell NPs. The *I-V* and *C-V* characteristics were examined in a wide range of illumination intensities, wavelength (365 nm to 880 nm), and temperature (45 K to 292 K). The devices exhibit NPC at temperatures above 273 K as well as memory properties in both the I-V and C-V. The latter does not occur in similar devices with other metal NPs. The origin of the NPC is by excitation in the Co_3O_4 shell which lowers the free carrier density and hence the conductivity of the MIS structure. The maximum current reduction is observed for illumination in the 735–780 nm wavelength range. The NVM window increases with illumination as in devices with other metal NPs. The various functionalities varieties of the structure we described are not only important findings but can also serve as NVM MIS structures, with embedded semiconductor or metal NPs. Moreover, the ability of Co included materials to be magnetized in contrast with semiconductor or noble metal NPs, can potentially enlarge the functionality of the suggested device.

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