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Self aligned hysteresis free carbon nanotube field-effect transistors

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Hysteresis phenomenon in the transfer characteristics of carbon nanotube field effect transistor (CNT FET) is being considered as the main obstacle for successful realization of electronic devices based on CNTs. In this study, we prepare four kinds of CNTFETs and explore their hysteretic behavior. Two kinds of devices comprise on-surface CNTs (type I) and suspended CNTs (type II) with thin insulating layer underneath and a single global gate which modulates the CNT conductance. The third and fourth types (types III and IV) consist of suspended CNT over a metallic local gate underneath, where for type IV the local gate was patterned self aligned with the source and drain electrodes. The first two types of devices, i.e., type I and II, exhibit substantial hysteresis which increases with scanning range and sweeping time. Under high vacuum conditions and moderate electric fields ($|E| > 4 \times 10^6$ V/cm), the hysteresis for on-surface devices cannot be eliminated, as opposed to suspended devices. Interestingly, type IV devices exhibit no hysteresis at all at ambient conditions, and from the different roles which the global and local gates play for the four types of devices, we could learn about the hysteresis mechanism of this system. We believe that these self aligned hysteresis free FETs will enable the realization of different electronic devices and sensors based on CNTs. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4947099]

For more than a decade, single-wall carbon nanotubes (CNTs) have been considered as realistic alternative for conventional transistors.[1–6] Substantial efforts were devoted for either growing or positioning the tubes at specific locations for functional operations.[7–12] Other efforts demonstrated different electrical components, such as inverters, memory cells, and logic circuits based solely on CNTs.[13–16] One may assume that full integration of CNTs within silicon technology can be realized in few years. However, for efficient operation of any commercial electronic circuit each component should have reproducible electrical performance and low noise level. Due to the superb sensitivity of CNTs to their external environment, these two crucial requirements are far from being fulfilled.

On-surface CNTs are known to suffer from low signal to noise ratio (SNR) due to charged traps within the insulating medium, and fabrication residues, such as PMMA and photoresist.[14,15,17–21] Suspended CNTs have much higher SNR, especially if are grown at the last step of the fabrication process.[22,23] Yet, these suspended CNTs exhibit significant hysteresis in their transfer characteristics at ambient conditions, which depends on the scan rate and on the gate voltage range.[24–27] Commercial application such as chemical sensing,[28,29] which is considered as one of the most attractive applications of CNT field effect transistors (FETs), suffers dramatically from this phenomenon. The effective electric potential that governs the tube conductance tends to drift with time and a significant reduction of the device transconductance, and hence its sensitivity, occurs.

It was argued that few monolayers of water are responsible for this hysteresis. In a recent study, Pascal-Levy *et al.*[25,27] reported that these monolayers of water on the oxide film assist back gate (i.e., global gate) screening by mobile charges, and behave as resistor-capacitor (RC) circuit,[30] with relaxation time which is inversely proportional to the oxide conductivity. This phenomenon causes retardation in the electrostatic environment which affects the CNT conductance and results in an uncontrollable hysteresis in the CNT transfer characteristics. Several studies have tried to minimize the hysteresis window, but none of them succeeded to eliminate it completely at ambient conditions.[22,31–34] In this letter, we present an alternative device geometry, based on a self aligned local metallic gate, which overcomes this obstacle, and achieves hysteresis free CNT FETs at ambient conditions. We describe the influence of the global and the local gates when they are gated separately, and when they are swept together in order to obtain deeper understanding of the hysteresis phenomenon.

In this study, four types of CNT FETs were prepared utilizing the growth at the end technique[22,23] in order to avoid any process residual contamination. One kind of devices (type I) comprises on-surface CNTs, and the other three comprise suspended tubes. Types I and II devices have thin insulating layer (SiO_2) underneath the CNTs and a single global gate which modulates the CNT conductance. Types III and IV consist of suspended CNTs over a metallic local gate underneath, where for type IV the local gate was patterned self aligned with the source and drain (SD) electrodes.

The processing was performed on 500 nm SiO_2 thermally grown on highly p-doped silicon substrate, using only photolithography techniques. First, SD were patterned with 5/40 nm Cr/Pt electrodes, with gaps of 1.3/1.8 μm between SD. Next, three types of trenches were fabricated. For types II and IV, 400 nm and 100 nm deep trenches were etched in 1:6 buffer oxide etch (BOE) for four and one minutes, respectively. For type III, the 400 nm trench was prepared by reactive ion etching (RIE). For types III and IV, additional lithography step was involved in order to deposit a thin

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metallic electrode (5/40 nm Cr/Pt) within the trench in between the SD electrodes (see Figs. 1(a)–1(d)). This metallic electrode serves as a local gate for types III and IV CNT FETs. For type IV, this lithography step included overlap of the local gate with the metallic SD electrodes resulting in a self aligned configuration. Finally (for all the devices), ferritin solution was deposited at specific places, and the CNTs were grown by chemical vapor deposition (CVD) with methane/hydrogen gas mixture (0.5/0.5 SLM) at 900 °C.[25,27]

Fig. 1(e) in the main text and Fig. S1 in the supplementary material[35] depict the transfer characteristics of CNT FETs in linear and logarithmic scales, respectively, one from each type (Figs. 1(a)–1(d)). All the measured devices comprise semiconducting CNTs with I_{ON}/I_{OFF} ratios larger than 10^2. From the linear part of the I-V_g curve (Fig. 1(e)), the linearly extrapolated crossing point (V_{on}) with the V_g axis (zero current) was measured, and the threshold voltage was extracted according to the following relation,[36] $V_{th} = V_{on} - V_{ds}/2$. For each sweeping direction, we obtained the respective threshold voltage, and the difference between the two values is noted as the hysteresis window, ΔH. At ambient conditions, type I and II CNT FETs exhibit an advanced hysteresis (counter clock wise - CCW, Fig. 1(e)). This hysteresis depends on the humidity level, gate voltage ranges, and sweep rates. Example for this behavior is presented in Fig. 2 where ΔH is plotted versus the different scanning ranges of the global gate voltage ($|V_{gg}|$) for both on-surface (I) and suspended (II) CNT FETs. At ambient conditions and humidity level of 60%, both I and II CNTs display an increase of the hysteresis window as the applied voltage range increases. However, at high vacuum

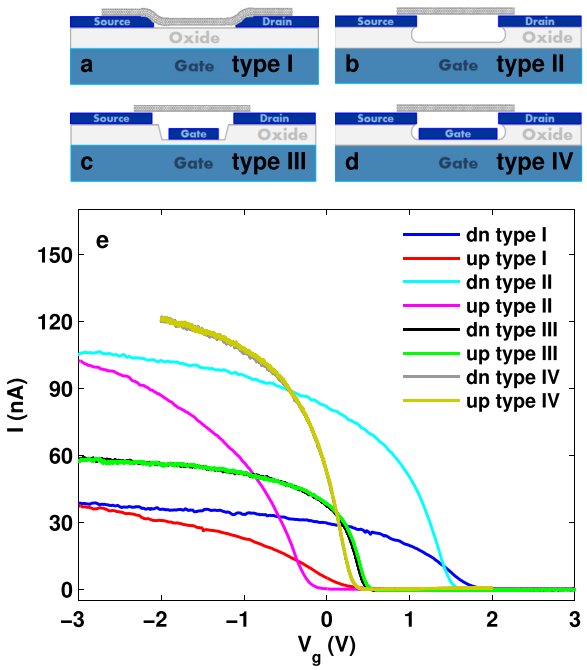

FIG. 1. Schematic diagrams of the four types of devices that were tested. (a), (b) On-surface (type I), or suspended (type II) CNTs with global gate, (c), (d) suspended CNTs with local gate (type III), or self aligned local gate (type IV) and global gates (for both III and IV), (e) transfer characteristics of type I (blue line-down, red line-up), type II (light blue line-down, magenta line-up), type III (black line-down, green line-up), and type IV (gray line-down, yellow line-up) CNT FETs. The curves were measured at ambient conditions, humidity level of 60%, and bias (V_{ds}) of 10 mV.

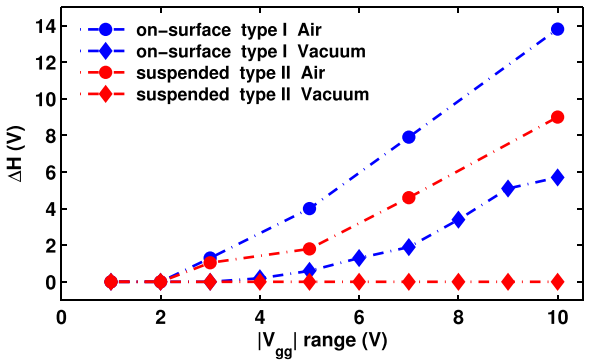

FIG. 2. Hysteresis window versus global gate sweeping ranges. Blue (red) circles present ΔH for type I (II) devices measured at ambient conditions with 60% humidity level. Blue (red) diamonds present ΔH for type I (II) devices measured at high vacuum ($<10^{-5}$ Torr).

conditions ($<10^{-5}$ Torr) where water vapor is absent, different behavior is found. At low gate sweeping ranges ($|V_{gg}| < 3$ V) which are equivalent to low up to moderate electric fields ($|E| < E_{cr} = 4 \times 10^6$ V/cm), both types I and II devices exhibit no hysteresis in their transfer characteristics. However, as the sweeping voltage range increases, hysteresis of I starts to develop as opposed to II where no hysteresis is visible for the whole sweeping range.

The reason is the following: at low gate sweeping ranges and ambient conditions, the source of hysteresis is few monolayers of water which adsorb to the oxide surface and assist charges redistribution in response to the external gate voltage. When vacuum is introduced, water vapor disappears and no hysteresis prevails. However, for higher sweeping ranges, charges can tunnel between the CNT and the oxide traps and the hysteresis reappears. For suspended tubes, this back and forth tunneling is prevented, and no hysteresis is possible. This fundamental result states that even if one passivates a CNT FET beside the reduction of the SNR of the outcome device, the hysteresis will reappear at moderate and high electric fields.

Hence, hysteresis free CNT FETs, which typically operate at moderate and high electric fields, can not rely on on-surface devices but only on suspended ones. However, at ambient conditions even the suspended CNT devices suffer from hysteresis, as evident from previous studies and Figs. 1(e) and 2. Since the source of hysteresis for suspended CNTs originates from water assisted surface charge redistribution on top of the oxide layer, and because the hysteresis time constant of the equivalent resistor-capacitor (RC) circuit is proportional to $1/\sigma_{ox}$, where σ_{ox} is the oxide surface electrical conductivity,[25,27] an alternative device layout should be considered. Two architecture alternatives are types III and IV devices, where the CNT is suspended not over an oxide surface but rather over a local metallic gate. Figs. 1(e) and S1[35] depict the transfer characteristics of these devices as well (types III and IV), and clearly a substantial improvement in ΔH is observed. Type III device shows significant reduction of the hysteresis, and for device IV it is completely eliminated.

Interestingly, the hysteresis window and direction (clock wise (CW) or CCW) depend on the role of the local and the global gates during the measurements. In previous

reports,[25,27] we have confirmed that different sweep rates sample the temporal evolution of the hysteresis. Thus, in order to study further the influence of the metallic gates, we measure the hysteresis window at different sweep rates for different setups of the local and global gates. Fig. 3 depicts the results of these measurements. In order to present CCW and CW hysteresis in the same plot, we denote CCW hysteresis as positive ($\Delta H > 0$, advanced hysteresis[25]) and CW hysteresis as negative ($\Delta H < 0$, retarded hysteresis[37]). The red symbols present the hysteresis window when one sweeps V_{gg} and $V_{lg} = 0$ (right axis). The green symbols present the hysteresis window when one sweeps V_{lg} and $V_{gg} = 0$ (left axis). We denote these two configurations *A* and *B*, respectively. The blue symbols correspond to measurements where the two metallic gates were connected and swept together (configuration *C*, left axis). First, we notice that for types III and IV, the resulting ΔH for the three tested configurations is substantially smaller than those depicted in Figs. 1(e) and 2 for device types I and II. Second, as was mentioned before, configuration *C* yields the minimal $|\Delta H|$ for both III and IV, which vanishes completely for type IV device at low sweep rates. Additionally, $\Delta H < 0$ (CW) for configurations *B* and *C*, and $\Delta H > 0$ (CCW) for *A*.

Careful examination reveals the following observations: (a) minimizing the exposed oxide surface in the vicinity of the CNT reduces $|\Delta H|$; (b) reducing the electrostatic coupling between the global gate and the CNT decreases the hysteresis

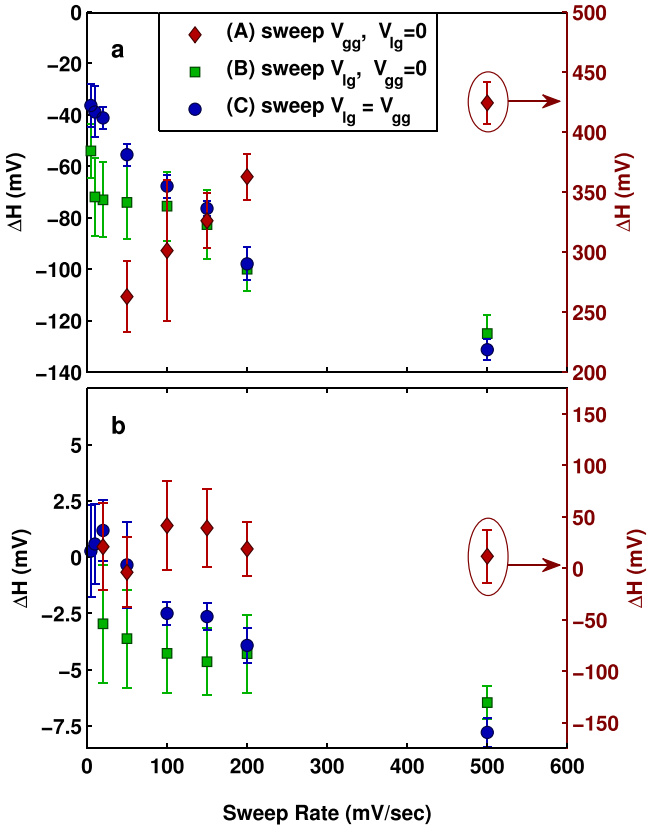

FIG. 3. Hysteresis window, ΔH, as a function of sweep rate for the different device types and configurations. The different symbols for the different device configurations are marked in the figure legends. (a) ΔH for device type III: configuration *A* (red) - right axis (red), configurations *B* (green) and *C* (blue) - left axis. (b) ΔH for device type IV: configuration *A* (red) - right axis (red), configurations *B* (green) and *C* (blue) - left axis.

window. In order to elucidate the last point, we measure the mutual capacitance between the global (local) gate and the tube $C_{gg}(C_{lg})$ for device types III and IV. Fig. S2a(b)[35] depicts the conductance (G) of a CNT as function of both V_{lg} (x-axis) and V_{gg} (y-axis) for device type III(IV). The ratio C_{lg}/C_{gg} is extracted from the slops of equi-conductance contours (white dashed lines). As expected, for device type III this ratio is ≈5, where for device type IV it is much larger, approaching ≈74.

This substantial difference between the two capacitance ratios can be easily understood from the three insets of Fig. S2.[35] The inset of Fig. S2(a)[35] presents scanning electron microscopy (SEM) image of type III fabricated device. The local gate is located between the two upper and lower SD electrodes and a faint CNT is bridging the gap over the predefined trench. As observed, two narrow oxide rims are located between the local gate and the two electrodes. The electric field originated from the global gate is screened by the metallic local gate, but not entirely due to the two oxide rims. As a consequence, the mutual capacitance between the global gate and the tube (C_{gg}) is not negligible. However, the case for type IV is different. The right inset of Fig. S2(b)[35] presents a top view of an SEM image of type IV device and a CNT bridging the gap (yellow arrow). Clearly, the two earlier mentioned oxide rims are absent, and the local gate spans over the entire trench area up to the SD electrodes. The left inset presents an SEM image of the cross section of a cleaved device. From this image, we can see that the metallic local gate is indeed self aligned with the two SD electrodes, and its edges lay underneath both electrodes without causing any shorts. This alignment is responsible for the almost complete screening of the global gate by the metallic local gate and to the high capacitance ratio of this device type.

Next, we address the physical mechanisms for the hysteresis phenomenon as implied from our data. As previously discussed, moisture is responsible for the hysteresis phenomenon in device types I and II. For device type III, two sources for the ΔH exist: (a) narrow oxide rims that can adsorb moisture which give rise to CCW hysteresis similar to I and II (which increases with reducing the sweep rate of the global gate), and (b) charge tunneling between shallow traps within the oxide layer and the adjacent metallic local gate edges.[37] For configuration *A*, in which the local gate is grounded and the sweeping voltage is applied to the global gate, strong electric fields exist between the two gates and charge tunneling between the local gate and the oxide traps is enabled.[38] These traps cause CCW hysteresis which decreases with reducing the sweep rate. The lifetime of electrons within the shallow traps is short and for slow sweep rates, the charge imbalance between upwards and downwards sweeping gate voltage is much smaller than for faster sweep rates. The data of the *A* configuration in Fig. 3(a) support the second mechanism as the dominant contribution for ΔH. On the other hand, few other devices of type III exhibit the dominance of the first mechanism. For such cases, the $\Delta H > 0$ (CCW) and increases with slower sweep rates.

For configuration *B*, in which the global gate is grounded and the local gate is swept, similar charge tunneling processes are feasible; however, this time they contribute CW hysteresis for type III devices. In configuration *A*, the sweeping voltage (V_{gg}) is below the oxide traps, resulting in

CCW hysteresis, where for the *B* configuration the sweeping voltage (V_{lg}) is above these traps, resulting in CW hysteresis. In this configuration, the moisture mediated hysteresis is significantly reduced due to the fact that surface charge redistribution is much less effective in screening the electric fields originated from the local gate as opposed to strong screening efficiency in configuration *A*. Indeed, the data of the *B* configuration in Fig. 3(a) reflect CW hysteresis, however, approximately four times smaller in magnitude than the same data for *A*. This reduction in the hysteresis window is attributed to the stronger electrostatic coupling of the local gate to the tube in comparison to the global gate ($C_{lg}/C_{gg} \approx 5$). In an attempt to eliminate these charge tunneling processes, one should impose the same electrical potential on the two metallic gates, i.e., $V_{gg} = V_{lg}$ (configuration *C*). Indeed, it results in the lowest $|\Delta H|$ among the three studied configurations for device type III. Although the hysteresis window for *C* is very small at low sweep rates, it does not disappear completely. This small residual hysteresis originates from charge transfer between the metallic local gate and the oxide traps as a consequence of the high electric fields which exist between the local gate and the SD electrodes.

Type IV device was designed in order to overcome these obstacles. The self aligned local gate eliminates any oxide rims adjacent to it, and disables any influence of charge tunneling as a consequence of electrical potential differences between the local gate and the SD electrodes for configuration *C*. A direct consequence of this configuration is an almost perfect screening of the global gate by the metallic local gate, as evident from the high capacitance ratio $C_{lg}/C_{gg} \approx 74$ (Fig. S2(b)[35]). As expected, all of the three configurations (*A*, *B*, and *C*) yield much smaller $|\Delta H|$ in comparison to their analogs in device type III. Even though it is CW for *C*, it is merely a consequence of the measurement setup ($\Delta H \approx \nu \times \tau$, where ν is the sweep rate in mV/s and $\tau \approx 30$ ms is the integration time constant of the measurement setup. This additional hysteresis window is always negative and can be reduced completely by lowering the sweep rate and/or reducing the measurement time constant). Hence, we can safely claim that below sweep rate of 200 mV/s, $|\Delta H| < 5$ mV, and practically disappears completely as the sweep rate reduces. These results are superior to those presented by Cao *et al.*[22] and Muoth *et al.*[31] In Ref. 22, the authors fabricated similar structure to device type IV; however, they succeeded to eliminate completely the hysteresis window only at specific environments, such as dry air, argon, or vacuum, and not in ambient conditions. In Ref. 31, the authors developed a complex fabrication process of CNT FETs which involved shadow mask evaporations and needle like formation of the electrical contacts to the CNTs. However, the resulted CNTs were quite resistive and the smallest measured hysteresis window was $\Delta H = 8 \pm 5$ mV at 4 mV/s. Our fabrication method is much simpler, easy to scale-up, and results in vanishing of the hysteresis window even for much larger sweep rates.

In summary, four types of devices were presented in order to elucidate the dominant hysteresis mechanisms of CNT FETs. Type I comprises on-surface CNT, and type II comprises suspended CNT. Both types have single global gate and SiO_2 layer underneath the CNTs. Types III and IV comprise suspended CNTs as well but over a predefined local metallic gate additionally to the global back gate. For type IV, the local metallic gate was patterned self aligned with the SD electrodes. At ambient conditions, device types I and II exhibit substantial hysteresis window (ΔH) which cannot be eliminated. The main source for the hysteresis phenomenon is water assisted mobile charge redistribution on top of the oxide layer. Hence, utilizing local metallic gates should diminish this effect substantially, as measured by device types III and IV. However, due to charged traps within the oxide layer in the vicinity of the local metallic gate edges additional source of hysteresis prevails and prohibits complete elimination of ΔH. Device type IV overcomes this obstacle and the resulted ΔH vanishes.

We believe that device type IV which succeeds to overcome all the mentioned obstacles can serve as essential prototype for ultra sensitive chemical sensors and alternative electrical devices based on CNT FETs.

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