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High performance horizontal gate-all-around silicon nanowire field-effect transistors

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Abstract

Semiconducting nanowires have been pointed out as one of the most promising building blocks for submicron electrical applications. These nanometer materials open new opportunities in the area of post-planar traditional metal–oxide–semiconductor devices. Herein, we demonstrate a new technique to fabricate horizontally suspended silicon nanowires with gate-all-around field-effect transistors. We present the design, fabrication and electrical measurements of a high performance transistor with high on current density ($\sim$150 μA μm^{-1}), high on/off current ratio (10^6), low threshold voltage (~ -0.4 V), low subthreshold slope ($\sim$100 mV/dec) and high transconductance ($g_m \sim 9.5$ μS). These high performance characteristics were possible due to the tight electrostatic coupling of the surrounding gate, which significantly reduced the Schottky-barrier effective height, as was confirmed experimentally in this study.

(Some figures may appear in colour only in the online journal)

1. Introduction

Metal–oxide–semiconductor (MOS) technologies have been improved at an unprecedented rate during the last four decades. The most significant progress was mainly due to the ability to preserve the minimization skills in the semiconductor industry, with no significant modification of the basic device structure. However, many new challenges such as gate oxide scaling, short channel effects and excessive power dissipation are limiting the continuity of this progress, threatening the stability of this trend in the future.

In order to keep the minimization capabilities, new approaches ought to be considered. Quasi-one-dimensional semiconducting structures have been widely investigated as a potential candidate for submicron electronic application. These nanowires (NWs) are expected to reduce the short channel effect (SCE) and drain induced barrier lowering (DIBL), and to possess optimal subthreshold slope (SS) of $\sim$60 mV/dec, and high transconductance. However, lack of doped source and drain contacts in most of these devices deteriorates their performance with respect to theoretical estimations. For example, for bottom-up silicon nanowires (SiNWs) nickel silicide contacts are commonly used and Schottky-barrier (SB) source and drain contacts are usually obtained. The barrier height is not negligible, and is found to be $\sim$0.67 eV and $\sim$0.4 eV for electrons and holes respectively [1, 2]. However, tight confinement of the electrical potential perpendicular to the wire axial direction may narrow the SB along the current direction and decreases the contact resistance significantly [3, 4].

This approach was realized both with silicon on insulator (SOI) based SiNWs and with NWs that were synthesized by the chemical vapor deposition (CVD) technique. Solutions such as double gate, FinFET, and Ω gate improved dramatically the transistor performance [5]. The ultimate electrostatic confinement of gate-all-around (GAA) was realized for top-down SOI based SiNWs [6], and presents almost ideal SS, low DIBL, and high I_{on}/I_{off} ratios. This study presented excellent device behavior for SOI NWs with implanted boron or arsenic source and drain contacts; however, this process is complicated and demands perfect alignment between the source and drain electrodes and

the surrounding gate. In subsequent study the same group presented SOI NWs with GAA with nickel silicide source and drain contacts [4]. Although these FET characteristics are slightly reduced with respect to the previous ones, the fabrication process is well controlled and it is much easier than before. The main advantage of these FETs arises from the low or even zero effective SB height as was confirmed from thermal activation analysis. This negligible barrier is a consequence of the tight electrostatic confinement created by the surrounding gate.

This approach looks very promising; however, there are a few limitations in this process. The surrounding gate was built from deposition of polysilicon, implantation of phosphorus, and activation at 1050 °C for 10 s. These high temperature processes restrict the flexibility of this method in being adopted for different NWs that cannot sustain such high temperatures, and for different stages of integration with current CMOS technology.

GAA configuration was also realized for vertically aligned grown SiNWs. These structures are very challenging to fabricate and device performances were inferior to those found using SOI NWs. The main disadvantage arises from having part of the channel without gate coupling and as a result higher contact resistance, and lower transconductance. These serious limitations may cause disqualification of numerous electronic applications and severely complicate the traditionally planar circuit design. Nevertheless, the appeal of a surround gate NW composed of an ultrathin semiconductor with low surface deformations functioning as a three dimensional FET is still extant. The necessity for a more efficient and economic method that allows careful engineering of a single NW device as well as the ability to manufacture numerous devices on a wide area is a desirable solution.

To address these issues, we demonstrate an alternative technique to produce horizontal gate-all-around nanowire FETs (HGAA-NWFETs). The method exploits horizontally suspended SiNWs (grown by a CVD tool) with a thin SiO_2 insulating layer and metallic gate deposited all around. Nickel–silicide source and drain contacts have been produced and the intrusion silicide segments penetrate underneath the gate area, thus insuring efficient gate coupling for the whole channel length. Although these kinds of FET should belong to SBFETs, the effective barrier height was reduced significantly by the efficient gate coupling as will be analyzed and discussed below. The device performance is impressive as well: hole mobility of 140 $cm^2\ V^{-1}\ s^{-1}$, SS in the range of 90–120 mV/dec, high on current values, and high transconductance, $g_m \sim 9.5\ \mu S$, which scales to $\sim 320\ \mu S\ \mu m^{-1}$ with the wire diameter. To the best of our knowledge, this is the highest g_m per unit length that has been measured in bottom-up SiNWs of similar channel lengths. The device fabrication, electrical measurements, theoretical model, and analysis are described below.

2. Experimental details

The silicon nanowires were synthesized by the VLS method in an ultrahigh vacuum chemical vapor deposition (UHV–CVD) chamber, with silane as the silicon precursor and gold as the catalyst [7, 8]. The growth temperature was 420 °C, and wires were lightly p doped with diborane precursor. A 2 nm thick gold film that was deposited on a Si(111) substrate was used to form gold catalyst droplets by agglomerating when annealed at 450 °C for 10 min prior to initiation of the growth. The nanowires were grown in ⟨112⟩, ⟨110⟩, and ⟨111⟩ directions with typical diameters of 35–60 nm, 25–40 nm, and above 50 nm, respectively. The gold catalyst was removed from the nanowire tip by etching the nanowires in a commercial gold etchant (a KI–I_2 based solution), and the SiNWs were oxidized in CVD reactor at 700 °C for 90 min in oxygen atmosphere with a flow rate of 100 sccm and pressure of 1 atm, resulting in a uniform silicon dioxide shell of $t_{ox} \sim$ 5–10 nm, wrapping the entire SiNW, as was confirmed from transmission electron microscopy (TEM) and depicted in figure 1(a).

The process flow we have used is sketched in figure 2. After oxidation, the SiNWs were randomly dispersed from an ethanol suspension onto highly doped silicon substrate capped by a 100 nm of dielectric layer of Si_3N_4 that was precovered with a 100 nm polymethylmethacrylate (PMMA) layer, that serves as a sacrificial layer. Unlike common NW device fabrication strategy, where the source and drain were defined before the gate, here, in order to have GAA, we replaced this order. A second layer of PMMA was spun again, and electron beam lithography was used to define the gate with the desired channel length, followed by 30/170 nm of Cr/Au metal evaporation. In order to achieve fully radial and symmetrical grip of the NWs by the gate electrode, the sample was placed during the evaporation on a home-made rotating and tilted stage. Figure 1(b) presents a high resolution scanning electron microscopy (HRSEM) image of a focused ion beam (FIB) lamella of SiNW after gate evaporation. The black circle in the middle of the image is the SiNW, and the white material is the metallic gate electrode. The image confirmed that metallic coating does indeed exist all around the circumference of the wire, as was required for GAA operation. Usually, GAA is realized via deposition of polysilicon, ion implantation, and a thermal annealing process, which limit the allowed NWs, and their integration process flow. The alternative method we have described is not restricted to a specific NW, and may be integrated at any stage with Si technology.

Next, source and drain (S/D) electrodes were patterned and Ni/Au metals (120/80 nm) were deposited with a similar tilting angle and rotating stage as for the gate stage. As a consequence, nickel atoms surrounded the silicon wire as well, and improved nickel silicide formation as will be described below. Before metal deposition, a 10 s etch in 1:6 buffered oxide etch (BOE) was performed to remove the thermal oxide shell of the SiNWs in the contact area region. The S/D and gate electrodes were designed to be distant enough to avoid any alignment limitation and lithography challenges. To bridge between the S/D electrodes and the wire segment that is confined by the gate, and to assure good Ohmic contacts to the wire, nickel silicide intrusions were formed. This idea of self-aligned formation of nickel silicide as metallic extended segments of the S/D electrodes

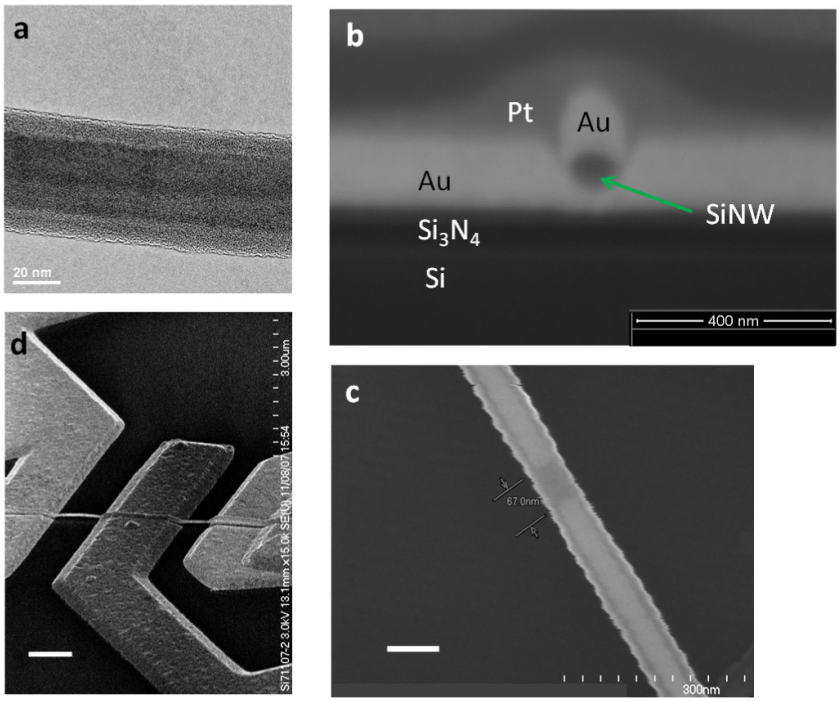

Figure 1. (a) TEM image of SiNW after thermal oxidation. (b) HRSEM cross section image of SiNW with metallic (Cr/Au) surrounding gate. The black circle is the SiNW cross section and the white parts below and above are the metallic (Cr/Au) surrounding gate. Platinum was deposited during the preparation of this cross section using a focused ion beam (FIB). (c) HRSEM image of SiNW with nickel silicide intrusion segments and channel length of ∼67 nm. The zigzag shape is due to interaction of the electron beam with the suspended wire. The scale bar is 100 nm. (d) Tilt-view SEM image of the HGAA-SiNW-FET device. The gate length is 1.5 μm, and the SiNW is hanging ∼100 nm above the silicon nitride substrate, gripped by the surrounding gate and the S/D electrodes. The scale bar is 1 μm.

was proven to be an efficient bridging solution [5, 9]. In order to reach the gated part of the wire, without shorts, the silicide phase formation process should be controlled and reproducible. In a recent paper [10], the authors study this process and conclude that the quality and oxide residues of the wire in the contact area may render this classical diffusion process into point contact diffusion, in which silicide formation rate is less predictable. Therefore, special care was taken to insure complete oxide removal in the contact area, no deficiency of Ni atoms in the S/D reservoirs, and a gentle rapid thermal annealing (RTA) process right after the Ni electrode liftoff. Since the annealing process was done after the device fabrication was completed, several annealing cycles were performed until the silicide segments reached the gated part of the wire. This overlap between the S/D silicide electrodes and the gated NW segment was electrically tested for each RTA cycle, until it was verified, and is crucial for obtaining high performance GAA-FETs. The fact that the silicide formation was well controlled enabled us to shrink the channel length to sub-100 nm lengths, without any complicated alignment procedure, as can be seen in figure 1(c), where the channel length is ∼67 nm. A scanning electron microscopy (SEM) image of a typical complete fabricated HGAA-SiNW device with 1.5 μm gate length is shown in figure 1(d). The SiNW hangs ∼100 nm above the silicon nitride substrate, gripped by the surrounding gate and the S/D electrodes.

The first PMMA layer functioning as a thin sacrificial buffer is a very convenient way to attain complex nanometer structures, using pre-grown semiconductor building blocks. The use of PMMA as the first layer enables straightforward integration with the e-beam lithography technique. Alternatively, one can use fluid-directed assembly or other large-scale hierarchical orientation techniques to produce large numbers of GAA devices over large areas, using the same principles with standard photoresist and photolithography. Additionally, it is worth noting that all the excess SiNWs that were not connected to any gate electrode, are washed away during the standard electrode liftoff process, leaving just the required functional devices on the uncontaminated wafer. This small advantage is of great help, taking into account the ability to replicate the process to produce more devices on the same chip, having no fear of undesired wire contamination that might cause short circuits, or change the operation logic. Lieber *et al* [11] used layer-by-layer assembly of nanowires to illustrate fabrication of 3D electronics. Their approach is well compatible with the current suggested one. Considering the great advantage of HGAA-NWFET structures to overall chip performance, the substantial potential of these two combined methods seems to be promising. As opposed to the direct vertical growth surrounding gate structure, our approach enabled integration of both n-type and p-type SiNWs or any 1D NWs simultaneously, simply by depositing different NW types with different functionality. Another important advantage of the method is the ability to localize the wires at variable heights above the substrate, simply by adjusting the sacrificial first PMMA layer to the desirable thickness. This could be useful to many other applications,

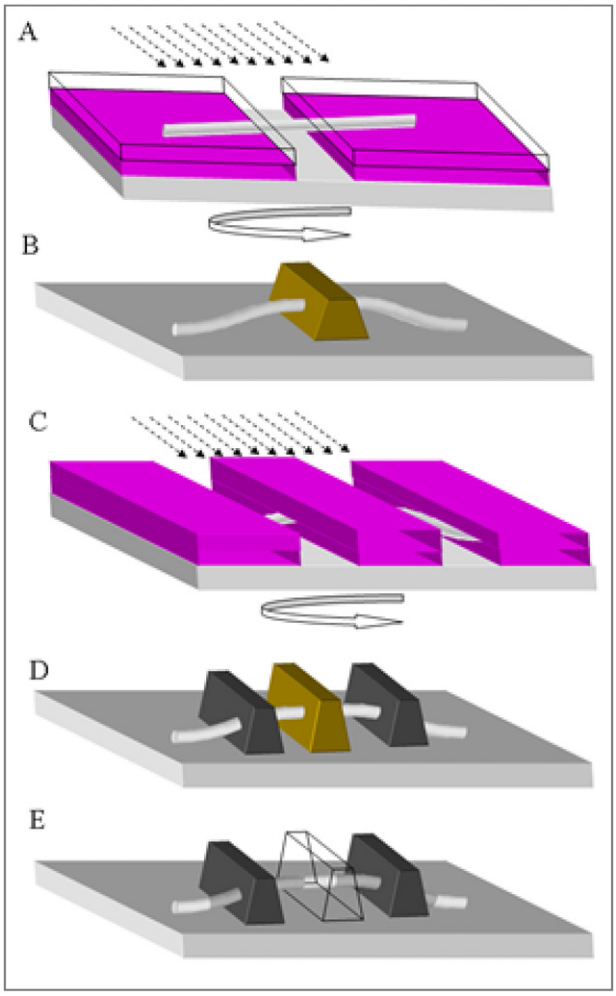

Figure 2. Schematic illustration of the fabrication steps of the HGAA-SiNW-FET. (A) The pre-oxidized silicon wires were spun onto a thin polymethylmethacrylate (PMMA) layer, 100 nm thick, and electron beam lithography was performed to pattern the top gate geometry. (B) A Cr/Au (30/170 nm) metal electrode was evaporated at a precalculated angle, using a rotating stage to achieve fully radial and symmetrical grip of the NWs by the gate electrode. (C) Second electron beam lithography was carried out to open the source/drain electrodes, located ∼600 nm apart from the middle of the top gate. (D) Nickel electrodes were evaporated in the same manner as the top gate, after oxide stripping with BOE at the contact areas. (E) Rapid thermal annealing (RTA) was performed at 420 °C for 60 s, resulting in nickel silicide formation along the ungated wire until the gated segment, enabling good overlapping between the S/D contacts and the surrounded gate electrode.

including nano-electro-mechanical systems (NEMS), as will be discussed elsewhere [12].

In addition, for device operation, the fact that the wires are suspended at the beginning of the fabrication process enables us to engineer residual stresses along the channel [13]. These stresses, either tensile or compressive, are known to modify the scattering time between the silicon sub-bands, and hence to change its electronic mobility. Tuning these stresses according to our needs may increase significantly the mobility of these SiNWs, and results in devices with superb electrical performance.

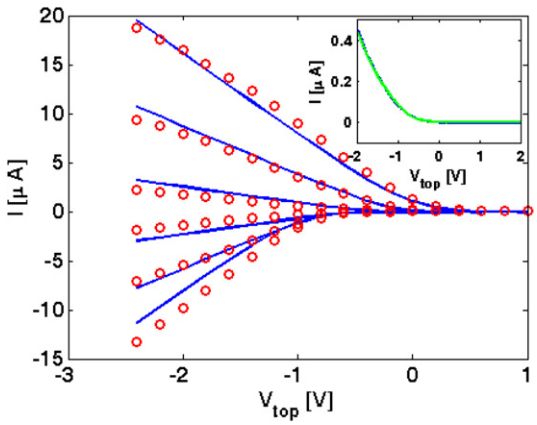

Figure 3. Transfer characteristics of device 1, with $L = 1.1\ \mu$m, $R_{si} = 18$ nm, and $t_{ox} = 7.5$ nm. In the main panel the blue lines present experimental data of I_{ds} versus V_{top} for different bias voltages of $V_{ds} = -1, -0.6, -0.2, 0.2, 0.6, 1$ V from bottom to top, respectively. Red circles present the theoretical fit according to equation (5), with the mobility as a single fitting parameter. Inset: no dependence of the current on the back gate voltage. I_{ds} versus V_{top} at $V_{ds} = -0.1$ V for several fixed back gate, V_{bg}, values, ranging from −10 V to 10 V with 4 V steps.

3. Results and discussion

Usually, SiNW SBFETs, based on nickel silicide S/D contacts, suffer from high resistance, low current, high SS (and not always constant), low transconductance, ambipolar behavior, and low I_{on}/I_{off} ratios. The main reason for these weaknesses arises from SB heights (SBHs) of $\phi_e \sim 0.67$ eV for electron transport, and $\phi_h \sim 0.4$ eV for hole transport, which hamper electron or hole transport to and from the NW. Hence, a great effort is exerted in order to reduce these effective SBHs as much as possible [14]. One possible solution is realized using GAA SiNWs [4]. Figures 3 and 4 present transfer characteristics of two different SiNW FETs with GAA (we shall denote this as top gate, V_{top}) fabricated as described before. These electrical measurements were performed at room temperature in ambient conditions. First, we excluded any current leakage through the oxide shell of the NWs between the top gate and the S/D electrodes. The measurements show neglected leakage current, less than 10 pA, which is in the range of the system noise level.

Next, we checked if there exists any current dependence on the external back gate voltage (V_{bg}) applied to the highly doped Si substrate. Measurements of I_{ds} versus V_{top} for several fixed back gate voltages (−10 to 10 V with 4 V steps) and a constant drain bias ($V_{ds} = 0.1$ V) demonstrated current independence and no influence of the back gate voltage, confirming the electrical screening of the SiNWs by the surrounding gate (inset of figure 3). Moreover, this electrical screening indicates that the extended S/D electrodes are fully silicided along the exposed (ungated) NW segments, operating as metallic contacts, and screen the back gate voltage as well. This measurement scheme was used to test and halt the silicide formation RTA cycles.

Returning to the experimental data, the main panel of figure 3 displays the current, I_{ds}, versus the top gate at

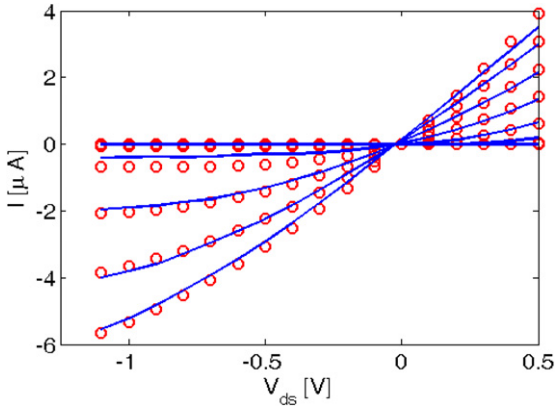

Figure 4. Transfer characteristics of device 2, with $L = 2.2\ \mu$m, $R_{si} = 20$ nm, and $t_{ox} = 10$ nm. The blue lines present experimental data of I_{ds} versus V_{ds} for different surrounding gate voltages of $V_{top} = -2.5, -2, -1.5, -1, -0.5, 0, 0.5, 1$ V from bottom to top, respectively. Red circles present the theoretical fit according to equation (5), with the mobility as a single fitting parameter.

different drain biases. This device exhibits p-type behavior, as expected, with large on current in the accumulation mode of the transistor. Notably, the hysteresis occurrence, which is quite common in NW-FETs using back gate and dual gate geometry, had significantly decreased and was almost unobserved on the wrapped around gated structures. Hysteresis behavior might be a crucial factor in the device performance, leading to uncertainty in its threshold voltage (V_{th}) and undesirable dependence on the voltage swing direction. Even though the problem was addressed before and might be resolved by proper passivation, these *in situ* oxidized SiNWs integrated with the HGAA technique offer a much more robust method to avoid this undesired phenomenon. It is worthwhile to point out that, even at the most negative top gate voltages that were permitted (before leakage current between the channel and the top gate occurred), the I_{ds} curves show just a weak sign of current saturation, indicating that the device is still in its linear regime and did not reach its maximum possible conductance, which is usually determined by its series contact resistance. From the maximum conductance, an upper estimate for the contact resistance, R_c, may be obtained. One finds $R_c < 25$ kΩ, which is scaled into contact resistivity of $\sim 0.1\ \mu\Omega$ cm^2 for NW core radii of 18 nm, as was verified from atomic force microscopy (AFM) and TEM measurements. This resistivity is extremely low, much lower than what is expected for SB contacts, and is comparable to ion implanted SiNW contact resistivities [15]. Moreover, for those devices that possess low contact resistance, from the data of I_{ds} versus V_{ds} (figure 4 and similar), no rectification was observed for $|V_{top}| > |V_{th}|$, and at positive and negative low V_{ds} linear behavior was found. The origin of this low contact resistance will be discussed later on.

To estimate the performance of these devices, the on-current (I_{on}) and off-current (I_{off}) were extracted by the suggested method of Chau *et al* [16], where 70% of V_{ds} below the threshold voltage, V_{th}, and 30% of V_{ds} above V_{th} mark the on/off state of the device respectively, determining the operation range of the gate swing (V_{dd}) around V_{th}. The method is a suitable manner for benchmarking new nanotechnology devices, and was often used in previous estimation of 1D carbon nanotube and semiconducting NW FET devices. The threshold voltage can be extracted from the linearly extrapolated V_{on} voltage, determined from the intercept of the tangent through the maximum slope point (linear transconductance) of the I_{ds}–V_{top} curve and the V_{top} axis, and is given by $V_{th} = V_{on} - V_{ds}/2$ [17]. All our fabricated HGAA-SiNW devices presented an enhancement-mode FET characteristic with low negative threshold voltage in the range of (−0.4)–(−0.8) V. The measured I_{on} taken at $V_{ds} = -1$ V ($V_{dd} = 1$ V), as depicted in figure 3, is 3 μA, reaching a maximum drain current (I_{max}) of 20 μA at $V_{top} = -2.5$ V, presenting a current density of $\sim 150\ \mu A\ \mu$m^{-1}. Though the on-state performances are very promising, still the transistor can be firmly turned off, displaying off current that is about 1 nA at $V_{ds} = -1$ V, reaching ∼50 pA for a strongly depleted transistor. The obtained I_{on}/I_{off} ratio for the limited swing operation of $V_{dd} = 1$ V is 10^3 and can reach more than 10^5 for the total GAA voltage swing. Extracting the maximum derivative of the drain current with respect to the top gate results in a relatively high transconductance (g_m) with a peak of $\sim 9.5\ \mu$S. Normalizing this result with the core diameter of the inner conducting SiNW, the I_{on} and g_m scaled values are 0.15 mA μm^{-1}, and 0.316 mS μm^{-1}, respectively. These normalized results present significant improvements compared to previously reported high performance top gated and back gated SiNW FETs of comparable lengths [9, 18, 19], and within the same order of magnitude as much shorter, state of-the-art planar silicon p-type MOSFETs [20].

Usually, for a SBFET the subthreshold slope (SS) is larger than the optimal SS of 60 mV/dec at room temperature. This results from the modulation of the SB effective height with the external gate voltage. A logarithmic plot of I_{ds} versus V_{top} indeed exhibits linear behavior in the subthreshold zone with SS ≃ 105 mV/dec (figure 5). Other fabricated devices possess similar SS in the range of 90–120 mV/dec as well. Several studies [2, 4, 21] discussed and confirmed the expected SS values for several configurations of SB SiNW FETs. The basic approximate expression for the SS of the SBFET is given by

$$S = \frac{k_B T}{q} \ln(10) \left(1 - e^{\frac{-d_T}{\lambda}}\right)^{-1}, \qquad (1)$$

where q is the absolute electron charge, d_T is the tunneling distance above which tunneling can be ignored, and λ is the electric potential screening length along the wire [21]. Several expressions exist for λ, mainly depending on gate configuration and where the potential along the radial direction was calculated. A common estimation for λ for a warped gate structure is given by

$$\lambda = \left(2R_{si} + 2\frac{\epsilon_{si}}{\epsilon_{ox}} t_{ox}\right) \Big/ 4.81. \qquad (2)$$

ϵ_{si} and ϵ_{ox} are the dielectric constants of the silicon core and the oxide shell, respectively, R_{si} is the silicon core radius, and t_{ox} is the oxide shell thickness. Under reverse bias the

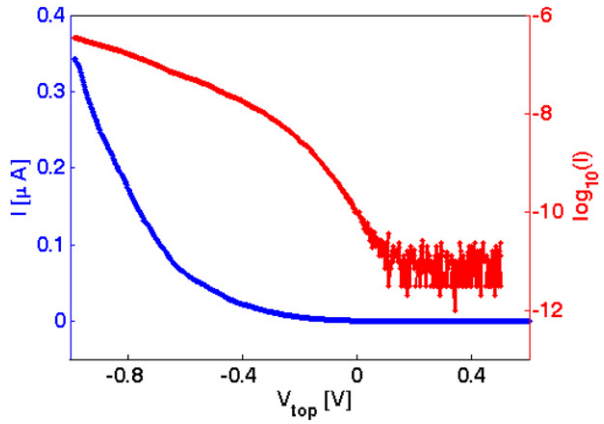

Figure 5. Linear (left) and log (right) scale plots of I_{ds} versus V_{top} at $V_{ds} = -0.5$ V. The extracted subthreshold slope is 105 mV/dec with $I_{on}/I_{off} \sim 10^5$ for the total top gate swing.

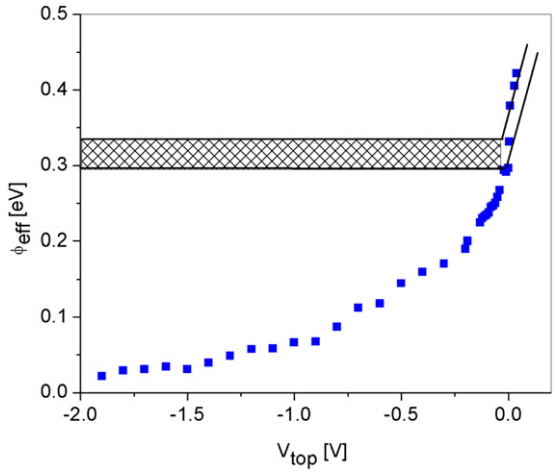

Figure 6. The effective SB height, ϕ_{eff}, versus the external surrounding gate, V_{top}, for device 1 as was derived in [22]. The intersection points between the horizontal stripe and the straight lines with slope 1 signify $\phi_o \approx 0.315 \pm 0.02$ V, and $V_{fb} \approx 0.0 \pm 0.05$ V.

potential shape of the SB is approximated by a triangular barrier, and using the Wentzel–Kramers–Brillouin (WKB) approximation one obtains the following implicit equation for d_T:

$$d_T = \frac{3\hbar}{2}\frac{\sqrt{\epsilon_{si}}}{\sqrt{2mq\phi_{SB}}}\frac{1}{\sqrt{1-e^{\frac{-d_T}{\lambda}}}}. \quad (3)$$

Using the measured t_{ox} and R_{si} one finds $\lambda = 17$ nm from equation (2), and $d_T = 4.65$ nm from equation (3). Plugging these two values back into equation (1) yields SS $\sim$ 250 mV/dec, which is much higher than the experimentally measured SS value. Since the SS value of equation (1) decreases as d_T increases, and d_T in turn increases as ϕ_{SB} decreases, one may conclude that the effective SB height is lower than the expected theoretical value. Below, we present experimental data of the SB heights that confirm this hypothesis.

Next, we present experimental result of I_{ds} versus V_{ds} for another (device 2) HGAA-SiNW-FET (see figure 4). The different curves are for different GAA voltages (V_{top}), and p-type FET behavior with strong saturation for negative bias on the drain electrode is observed. The curves display good linearity for both positive and negative small drain biases, corroborating the good Ohmic contacts for both S/D electrodes. The linearity of the curves near zero bias emphasizes the suppression of the nickel silicide conventional SBs as a result of the tight electrical confinement of the NW in the radial direction, and indicates that the transport is mainly determined by the NW channel itself. In order to verify this hypothesis the effective SB height, ϕ_{eff}, as a function of V_{top} should be measured. In a recent study [22] we present a detailed analysis of ϕ_{eff} versus V_{top} based on the method that was described in [3]. Briefly, we assume that at relatively large negative drain biases the current through the device can be modeled as

$$I_{ds} = A^* T^2 e^{-q\phi_{eff}/k_B T}, \quad (4)$$

where A^* is the Richardson constant, and ϕ_{eff} includes thermally assisted tunneling processes. When V_{top} is approximately the flat band voltage (V_{fb}), the expected barrier height should be $\phi_o \simeq 0.4$ eV. However, for negative gate voltages, the SB becomes thinner and thermally assisted tunneling processes are more accessible. As a result, the effective SB height extracted from the experimental data is reduced from its original value ϕ_o. From transfer characteristic data of device 1 for different temperatures between 4 K up to 300 K, we extracted ϕ_{eff}, and the main result of this analysis is plotted in figure 6, where ϕ_{eff} versus V_{top} is shown. Two main conclusions may be drawn from this plot. First, from the intersection points of the horizontal stripe with the straight lines with slope 1, as discussed in [3], $\phi_o \approx 0.315 \pm 0.02$ V and $V_{fb} \approx 0.0 \pm 0.05$ V can be extracted. Second, as expected, for gate voltages which are in the vicinity of V_{fb}, ϕ_{eff} is comparable to the known potential offset for holes at the interface between nickel silicide and silicon, $\phi_o \simeq$ 0.4 V. However, as the gate voltage decreases and becomes more negative, ϕ_{eff} monotonically decreases, until it becomes almost negligible for $V_{top} < -1$ V. Hence, the tight electrical confinement imposed by the surrounding gate indeed narrows the SB until it becomes almost transparent.

For $V_{top} < V_{th} \approx -0.4$ V, $\phi_{eff} < 0.15$ V which presents a significant reduction of ϕ_{eff} compared to ϕ_o, and may explain the device improved performance. For $V_{top} \geq V_{th}$ this effective barrier is not negligible and will deteriorate device performance, and Ohmic behavior. Similar results were found previously for top-down GAA SOI based SiNWs [4], where the SB effective height disappears completely for strong enough external gate. For grown SiNWs with nickel silicide contacts, previous studies demonstrated as well a reduction in the SB height, and ϕ_{eff} analysis as depicted in figure 6 verified this for the first time for bottom-up GAA SiNW FETs.

In order to compare the experimental data to a theoretical model two basic models are considered. The first attributes the wire resistance mainly to the NW itself, and the second is based on SBFET analysis. As mentioned before, for top gate voltages which are more negative than the threshold voltage, the effective barrier height is significantly reduced, and Ohmic

contacts may be assumed. In such a situation the current is given by [23] (with adjustment for hole carriers)

$$I_{ds} = \frac{4\pi\epsilon_{si}\epsilon_{ox}\mu_0}{L}\left(\frac{2k_BT}{q}\right)^2 (g(B_S) - g(B_D)), \quad (5)$$

where

$$g(B) = \frac{1}{2}\ln B + \frac{1}{B} - \frac{2\epsilon_{si}\epsilon_{ox}}{C_{ox}R_{si}}\frac{1}{B}\left(1 - \frac{1}{2B}\right). \quad (6)$$

C_{ox} is the GAA capacitance per unit area, μ_0 is the wire mobility, L is its length, and B_S and B_D are the solutions of the following equation for $V(x=0)=0$, and $V(x=L)=V_{ds}$, respectively:

$$\frac{q}{k_BT}\left(V(x) - (V_{top} - V_{fb}) - \frac{k_BT}{q}\ln\frac{8L_i^2}{R_{si}^2}\right) = f(B). \quad (7)$$

$L_i = \sqrt{\frac{k_BT}{q^2}\frac{\epsilon_0\epsilon_{si}}{n_i}}$ is the Debye screening length, n_i is the intrinsic carrier concentration, and $f(B)$ is given by

$$f(B) = \ln(1-B) - 2\ln B + \frac{4\epsilon_{si}\epsilon_0}{C_{ox}}. \quad (8)$$

In the linear regime above the threshold $f(B_S), f(B_D) \gg 1$, and therefore $B_S, B_D \sim 0$. As a result, $g \sim \eta/4B^2$, and $f \sim \eta(1-B)/B$, where $\eta = 4\epsilon_0\epsilon_{si}/C_{ox}R_{si}$. Plugging back these approximations into equation (8) and finding the solutions for B_S and B_D yields

$$\begin{aligned}\frac{\eta}{B_S} &= \eta - \frac{q}{k_BT}(V_{top} - V_0)\\ \frac{\eta}{B_D} &= \eta - \frac{q}{k_BT}(V_{top} - V_0 - V_{ds}),\end{aligned} \quad (9)$$

where

$$V_0 = V_{fb} - \frac{q}{k_BT}\ln\frac{8L_i^2}{R_{si}^2}. \quad (10)$$

Inserting equation (9) into (5) results in the following approximation for the current:

$$I_{ds} = \frac{2\pi\mu_0 C_{ox}R_{si}}{L}\left(V_{top} - V_{th} - \frac{1}{2}V_{ds}\right)V_{ds}, \quad (11)$$

where

$$V_{th} = V_{fb} - \frac{k_BT}{q}\ln\frac{8L_i^2}{R_{si}^2} + \frac{k_BT}{q}\frac{4\epsilon_0\epsilon_{si}}{C_{ox}R_{si}}. \quad (12)$$

Equation (11) resembles the usual current–voltage characteristics of a MOSFET, which predicts nonlinear behavior and current saturation, and provides an explicit expression for the threshold voltage, V_{th}. In order to compare our experimental data, either I_{ds} versus V_{top}, or I_{ds} versus V_{ds}, with the theoretical prediction of equation (5), several parameters need to be determined. The lengths and diameters of the wires were measured by AFM (atomic force microscopy). The total wire diameter can be expressed as $D = 2(R_{si} + t_{ox})$; since D is measured by AFM, having information on either the core radius or the shell thickness is sufficient for knowing the other parameter as well. From TEM images of our oxidized SiNWs we deduced that the oxide thickness, t_{ox}, is between 5 and 10 nm (see figure 1(a)). V_{fb} was measured, as was described before, using the analysis of the effective SB height versus gate voltage (see figure 6), and found to be $V_{fb} = 0 \pm 0.05$ V. V_{th} can be estimated from the intersection point, V_{on}, of the tangent to the linear part of the I_{ds} versus V_{top} curves with the x-axis, according to the following relation: $V_{th} = V_{on} - V_{ds}/2$. For device 1, $V_{th} = -0.4 \pm 0.05$ V, and after plugging it into equation (12) and solving for the wire core diameter one obtains $R_{si} = 18 \pm 3$ nm, and $t_{ox} = D/2 - R_{si} = 7.5 \pm 3$ nm. The hole mobility is given by the following equation:

$$\mu_0 = \frac{L}{2\pi C_{ox}R_{si}V_{ds}}\frac{dI_{ds}}{dV_{top}}, \quad (13)$$

and from the linear segments of the $I_{ds} - V_{top}$ curves the mobility is found to be $\mu_0 = 140 \pm 10$ cm^2 V^{-1} s^{-1}. First, it is worthwhile to mention that from the fact that $V_{fb} \sim 0$ V, and the small work function difference between the gate electrode (chromium) and the SiNW of $\delta W \approx 100$ mV, one can deduce that the trap density and the interface states are very low. Second, having all the required parameters, it is possible to compare the experimental data to equation (5). The red circles in figures 3 and 4 present the fitting according to equation (5) using the parameters of devices 1 and 2 respectively, and the mobility as a single fitting parameter. The agreement between experiment and theory is very good, which suggests that indeed the GAA creates a strong electrostatic confinement of the wire and causes a significant reduction of the SB effective height to such an extent that the transport behavior is mainly determined by the channel itself and not by the contacts. The outcome mobilities were 142 cm^2 V^{-1} s^{-1} and 145 cm^2 Vs^{-1} for devices 1 and 2, respectively, which are very close to the mobility values that were extracted from the experimental data according to equation (13).

All the devices that we have fabricated and measured so far were longer that 1 μm. However, due to the strong gate coupling, no SCE or DIBL is expected for channels that are ten times shorter. The channel length can be controlled very precisely by the nickel silicide intrusion process of the S and D electrodes (see figure 1(c)). As a result, according to equation (5), short channel HGAA-SiNW FETs are believed to operate much better even than presented in this study. Moreover, instead of using SiNWs as the building block, one can implement this method for more appealing materials such as Ge/Si heterostructure nanowires [24], pushing these already high performance devices to their limits.

4. Conclusions

In conclusion, an efficient way to produce bottom-up horizontal, gate-all-around, field-effect transistors was presented. This method is based on suspended SiNWs which are gripped by a metallic GAA, and nickel source and drain electrodes with nickel silicide intrusion segments that are penetrating beneath the surrounding gate. Transport characteristics of these initially made devices show extremely encouraging results, within the same order as planar silicon MOSFETs and a significant improvement with regard

to SiNW-FET devices with comparable channel length published to date.

The benefit of self-aligned diffusive metal silicide along the wire is an appealing strategy to achieve adjustable and controlled channel length. The weak point of this method, with respect to highly doped source and drain electrodes, is the formation of a Schottky barrier, resulting in early current saturation, which limits device performance. In this study, we demonstrate that the tight electrical coupling of the surrounding gate reduces these SB effective heights significantly, drives the contacts to Ohmic behavior, and enables the intrinsic silicon channel to determine solely the device electrical performance. We believe that the combined method of suspended wrapped around gate NWs and extended silicide electrodes is a promising way to accomplish high performance ultrasmall FET devices.

In addition, this robust method allows engineering flexibility at many levels, and opens a completely new direction, with many aspects which are still to be explored. For instance, it offers easy integration of different electrically characterized NWs simultaneously, good domination of a single device physical dimension, a competent alternative to achieve large numbers of devices over large areas, using previous developed techniques, and three-dimensionality lithography. We believe that the presented strategy will play an important role in future bottom–up nano-electronics.

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